# SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, AND SEMICONDUCTOR MOUNTING STRUCTURE


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| Patent Number: | JP2003347503 |
| Publication date: | 2003-12-05 |
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| Requested Patent: | JP2003347503 |
| Application Number: | JP20020156537 20020530 |
| Priority Number (s): | |
| IPC Classification: | H01L25/065; H01L21/60; H01L23/467; H01L23/473; H01L25/07; H01L25/18; H05K1/02; H05K1/14; H05K1/18 |
| EC Classification: | |
| Equivalents: | |



**Abstract**

PROBLEM TO BE SOLVED: To prevent a signal delay due to a wiring length and improve a heat radiation efficiency, in a semiconductor device or semiconductor module which is constructed into a three-dimensional structure by folding up a flexible wiring board.
SOLUTION: The semiconductor device or semiconductor module comprises the flexible wiring board which has bending sections and has a first principal plane (front principal plane) that can be mounted with a plurality of semiconductor chips at prescribed intervals; and at least one set of laminates composed of stacked semiconductor chips adjacent each other and mounted on the first principal plane (front principal plane) of the flexible wiring board, which is formed as a result of folding up the flexible wiring board at the bending sections, with wirings of the same function of the laminates being electrically connected by short cut wiring boards.

(19)日本国特許庁（ＪＰ）　　(12) **公開特許公報**（Ａ）　　(11)特許出願公開番号
特開2003－347503
（P2003－347503A）
(43)公開日　平成15年12月5日(2003.12.5)

| (51)Int.Cl.⁷ | 識別記号 | ＦＩ | テーマコード゛(参考) |
|---|---|---|---|
| ＨＯ１Ｌ　25/065 | | ＨＯ１Ｌ　21/60 | ３１１Ｒ　５Ｅ３３６ |
| 21/60 | ３１１ | | ３１１Ｗ　５Ｅ３３８ |
| | | ＨＯ５Ｋ　1/02 | Ｂ　５Ｅ３４４ |
| 23/467 | | 1/14 | Ｃ　５Ｆ０３６ |
| 23/473 | | 1/18 | Ｓ　５Ｆ０４４ |

審査請求　未請求　請求項の数16　ＯＬ　（全 17 頁）　最終頁に続く

(21)出願番号　特願2002－156537(P2002－156537)

(22)出願日　平成14年5月30日(2002.5.30)

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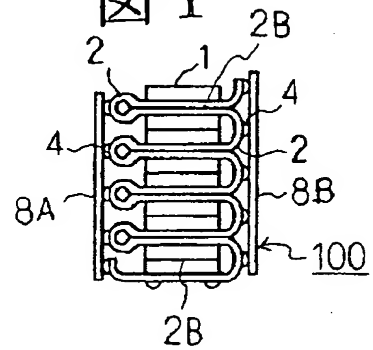
(54)【発明の名称】　半導体装置及びその製造方法並びに半導体実装方法

(57)【要約】
【課題】　可撓性配線基板を折り畳んで立体構造（三次元）にした半導体装置もしくは半導体モジュールにおいて、配線長による信号遅延を防止する。放熱効率を向上する。
【解決手段】　折り曲げ部を有し、複数の半導体チップが第１主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲部で折り曲げられて前記可撓性配線基板の第１主面（表主面）に搭載された隣合せの半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線をショートカット配線基板で電気的に接続した半導体装置もしくは半導体モジュールである。

図１



【特許請求の範囲】

【請求項１】　折り曲げ部を有し、複数の半導体チップが第１主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面に搭載された隣合せの半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線を電気的に接続するショートカット配線基板とを備えたことを特徴する半導体装置。

【請求項２】　折り曲げ部を有し、複数の半導体チップが第１主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面に搭載された隣合せの半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線を電気的に接続するショートカット配線基板と、前記可撓性配線基板の第２主面に設けられた前記積層体の同一機能の配線の共通端子と、該共通端子と実装基板の配線ランドとを電気的に接続する手段とを備えたことを特徴する半導体装置。

【請求項３】　折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第１主面に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第１主面に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカット配線基板で電気的に接続する工程とを備えたことを特徴する半導体装置の製造方法。

【請求項４】　折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第１主面に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第２主面に設けられた前記積層体の同一機能の配線の共通端子とを有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続する工程と、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第１主面に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカット配線基板で電気的に接続する工程と、前記共通端子と実装基板の配線ランドとを電気的に接続する工程とを備えたことを特徴する半導体装置の製造方法。

【請求項５】　折り曲げ部を有し、複数の半導体チップが第１主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面に搭載された隣合せの半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部とを備えたことを特徴する半導体装置。

【請求項６】　折り曲げ部を有し、複数の半導体チップが第１主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面に搭載された隣合せの半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部と、前記可撓性配線基板の第２主面に設けられた前記積層体の同一機能の配線の共通端子と、該共通端子と実装基板の配線ランドとを電気的に接続する手段とを備えたことを特徴する半導体装置。

【請求項７】　折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第１主面に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドと、前記積層体の同一機能の配線をショートカットするショートカット用配線接続部を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第１主面に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線のショートカット用配線同志を電気的に接続する工程とを備えたことを特徴する半導体装置の製造方法。

【請求項８】　折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第１主面に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第２主面に設けられた前記積層体の同一機能の配線の共通端子とを有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第１主面に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカットするショートカット用配線を電気的に接続する工程と、前記積層体の同一機能の配線の共通端子と実装基板の配線ランドとを電気的に接続す

る工程とを備えたことを特徴する半導体装置の製造方法。

【請求項９】　四つ折り曲げ部を有し、複数の半導体チップが第１主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面に搭載された半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部とを備えたことを特徴する半導体装置。

【請求項１０】　四つ折り曲げ部を有し、複数の半導体チップが第１主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面に搭載された半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部と、前記可撓性配線基板の第２主面に設けられた前記積層体の同一機能の配線の共通端子と、該共通端子と実装基板のランドとを電気的に接続する手段とを備えたことを特徴する半導体装置。

【請求項１１】　四つ折り曲げ部を有し、該四つ折り曲げ部で折り曲げられると、その第１主面に搭載される半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドと、前記積層体の同一機能の配線をショートカットするショートカット用配線接続部を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記四つ折り曲げ部で折り曲げて前記可撓性配線基板の第１主面に搭載された半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線のショートカット用配線同志を電気的に接続する工程とを備えたことを特徴する半導体装置の製造方法。

【請求項１２】　四つ折り曲げ部を有し、四つ折り曲げ部で折り曲げられると、その第１主面に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第２主面に形成された前記積層体の同一機能の配線の共通端子を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続する工程と、前記電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第１主面に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカットするショートカット用配線を電気的に接続する工程と、前記積層体の同一機能の配線の共通端子と実装基板のランドとを電気的に接続する工程とを備えたことを特徴する半導体装置の製造方法。

【請求項１３】　四つ折り曲げ部または折り曲げ部を有し、複数の半導体チップが第１主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部または折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面に搭載された半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した半導体装置であって、前記半導体チップが重ね合わされた積層体間に冷却路を設けたことを特徴とする半導体装置。

【請求項１４】　四つ折り曲げ部または折り曲げ部を有し、複数の半導体チップが第１主面に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部または折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面に搭載された半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線のショートカット用配線ランド同志を電気的に接続し、前記積層体の同一機能の配線の共通端子と実装基板のランドとを電気的に接続した半導体装置であって、前記半導体チップが重ね合わされた積層体間に冷却路を設け、前記可撓性配線基板の第２主面に前記積層体の同一機能の配線の共通端子を設け、該共通端子と実装基板の配線ランドとを電気的に接続したことを特徴とする半導体装置。

【請求項１５】　四つ折り曲げ部または折り曲げ部を有し、該四つ折り曲げ部または折り曲げ部で折り曲げられると、その第１主面に搭載される半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドと、前記積層体の同一機能の配線をショートカットするショートカット用配線接続部を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記四つ折り曲げ部または折り曲げ部で折り曲げて前記可撓性配線基板の第１主面に搭載された半導体チップを重ね合わされて積層する工程と、前記半導体チップが重ね合わされた積層体間に熱伝導性接着テープと熱吸収パッドで冷却路を形成する工程と、前記積層体の同一機能の配線のショートカット用配線同志を電気的に接続する工程とを備えたことを特徴する半導体装置の製造方法。

【請求項１６】　四つ折り曲げ部または折り曲げ部を有し、四つ折り曲げ部で折り曲げられると、その第１主面に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の

第２主面に設けられた前記積層体の同一機能の配線の共通端子を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第１主面に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記半導体チップが重ね合わされた積層体間に熱伝導性接着テープと熱吸収パッドで冷却路を形成する工程と、前記積層体の同一機能の配線をショートカットするショートカット用配線を電気的に接続する工程と、前記積層体の同一機能の配線の共通端子と実装基板のランドとを電気的に接続する工程とを備えたことを特徴とする半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、面実装型半導体装置もしくは半導体モジュール及びその製造方法に関し、特に、可撓性配線基板（フレキシブル配線基板）またはリードフレーム上に複数の半導体チップを搭載し、隣り合わせた半導体チップもしくは前記搭載された半導体チップを背中合わせにして重ね合せ、積層する技術に適用して有効な技術に関するものである。

【０００２】

【従来の技術】従来の小型化・高集積化を図る構造の半導体装置として、例えば、特開平９－１８１２１５号公報に記載されるように、可撓性配線基板（フレキシブル配線基板）の重畳部に半導体チップを組み込んだ封止体を有するとともに、可撓性配線基板の半導体チップ実装用外部端子（半導体チップ実装用ランド）が設けられた面の反対側面にも半導体チップを組み込んだパッケージ（封止体）を配置したものが提案されている（図２２～２４参照）。

【０００３】

【発明が解決しようとする課題】本発明者は、前記の従来技術を検討した結果、以下の問題点を見いだした。前記従来技術では、構造的には立体構造（三次元）で実装面積の小型化や高集積化が可能であるが、基板的には平面状（二次元）の基板を折り畳んだだけなので配線長は、通常の平面基板と変わりないため、配線長による信号遅延の問題があった。また、狭い空間に多数の半導体チップ（ＩＣチップ）等を積層したパッケージのため内部の熱が逃げにくく、動作不良等の問題があった。また、ＢＧＡ（Ball Grid Array）の半田ボール端子はリード端子と違い変形できないため、実装基板の変形や膨張によってクラック破断を起すという問題があった。

【０００４】本発明の目的は、基板を折り畳んで立体構造（三次元）にした半導体装置もしくは半導体モジュールにおいて、配線長による信号遅延を防止することが可能な技術を提供することにある。本発明の他の目的は、基板を折り畳んで立体構造（三次元）にした半導体装置もしくは半導体モジュールにおいて、放熱効率を向上することが可能な技術を提供することにある。本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述及び添付図面によって明らかになるであろう。

【０００５】

【課題を解決するための手段】本願において開示される発明の概要を簡単に説明すれば、以下のとおりである。第１の発明は、折り曲げ部を有し、複数の半導体チップが第１主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面（表主面）に搭載された隣合せの半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線を電気的に接続するショートカット配線基板とを備えた半導体装置である。

【０００６】第２の発明は、折り曲げ部を有し、複数の半導体チップが第１主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面（表主面）に搭載された隣合せの半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線を電気的に接続するショートカット配線基板と、前記可撓性配線基板の第２主面（裏主面）に設けられた前記積層体の同一機能の配線の共通端子と、該共通端子と実装基板の配線ランドとを電気的に接続する手段とを備えた半導体装置である。

【０００７】第３の発明は、折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第１主面（表主面）に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第１主面（表主面）に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカット配線基板で電気的に接続する工程とを備えた半導体装置の製造方法である。

【０００８】第４の発明は、折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第１主面（表主面）に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第２主面（裏主面）に設けられた前記積層体の同一機能の配線の共通端子とを有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体

チップの外部電極（パッド）とを電気的に接続する工程と、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第１主面（表主面）に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカット配線基板で電気的に接続する工程と、前記共通端子と実装基板の配線ランドとを電気的に接続する工程とを備えた半導体装置の製造方法である。

【０００９】第５の発明は、折り曲げ部を有し、複数の半導体チップが第１主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面（表主面）に搭載された隣合せの半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部とを備えた半導体装置である。

【００１０】第６の発明は、折り曲げ部を有し、複数の半導体チップが第１主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面（表主面）に搭載された隣合せの半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部と、前記可撓性配線基板の第２主面（裏主面）に設けられた前記積層体の同一機能の配線の共通端子と、該共通端子と実装基板の配線ランドとを電気的に接続する手段とを備えた半導体装置である。

【００１１】第７の発明は、折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第１主面（表主面）に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドと、前記積層体の同一機能の配線をショートカットするショートカット用配線接続部を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第１主面（表主面）に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線のショートカット用配線同志を電気的に接続する工程とを備えた半導体装置の製造方法である。

【００１２】第８の発明は、折り曲げ部を有し、該折り曲げ部で折り曲げられると、その第１主面（表主面）に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第２主面（裏主面）に設けられた前記積層体の同一機能の配線の共通端子とを有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第１主面（表主面）に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカットするショートカット用配線を電気的に接続する工程と、前記積層体の同一機能の配線の共通端子と実装基板の配線ランドとを電気的に接続する工程とを備えた半導体装置の製造方法である。

【００１３】第９の発明は、四つ折り曲げ部を有し、複数の半導体チップが第１主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面（表主面）に搭載された半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部とを備えた半導体装置である。

【００１４】第１０の発明は、四つ折り曲げ部を有し、複数の半導体チップが第１主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面（表主面）に搭載された半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した接続部と、前記可撓性配線基板の第２主面（裏主面）に設けられた前記積層体の同一機能の配線の共通端子と、該共通端子と実装基板のランドとを電気的に接続する手段とを備えた半導体装置である。

【００１５】第１１の発明は、四つ折り曲げ部を有し、該四つ折り曲げ部で折り曲げられると、その第１主面（表主面）に搭載される半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドと、前記積層体の同一機能の配線をショートカットするショートカット用配線接続部を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記四つ折り曲げ部で折り曲げて前記可撓性配線基板の第１主面（表主面）に搭載された半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線のショートカット用配線同志を電気的に接続する工程とを備えた半導体装置の製造方法である。

【００１６】第１２の発明は、四つ折り曲げ部を有し、四つ折り曲げ部で折り曲げられると、その第１主面（表

主面）に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第２主面（裏主面）に形成された前記積層体の同一機能の配線の共通端子を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続する工程と、前記電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第１主面（表主面）に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記積層体の同一機能の配線をショートカットするショートカット用配線を電気的に接続する工程と、前記積層体の同一機能の配線の共通端子と実装基板のランドとを電気的に接続する工程とを備えた半導体装置の製造方法である。

【００１７】第１３の発明は、四つ折り曲げ部または折り曲げ部を有し、複数の半導体チップが第１主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部または折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面（表主面）に搭載された半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線のショートカット用配線同志を電気的に接続した半導体装置であって、前記半導体チップが重ね合わされた積層体間に冷却路を設けた半導体装置である。

【００１８】第１４の発明は、四つ折り曲げ部または折り曲げ部を有し、複数の半導体チップが第１主面（表主面）に所定の間隔で搭載可能な可撓性配線基板と、該可撓性配線基板の前記四つ折り曲げ部または折り曲げ部で折り曲げられて前記可撓性配線基板の第１主面（表主面）に搭載された半導体チップが重ね合わされた少なくとも１組の積層体と、該積層体の同一機能の配線のショートカット用配線ランド同志を電気的に接続し、前記積層体の同一機能の配線の共通端子と実装基板のランドとを電気的に接続した半導体装置であって、前記半導体チップが重ね合わされた積層体間に冷却路を設け、前記可撓性配線基板の第２主面（裏主面）に前記積層体の同一機能の配線の共通端子を設け、該共通端子と実装基板の配線ランドとを電気的に接続した半導体装置である。

【００１９】第１５の発明は、四つ折り曲げ部または折り曲げ部を有し、該四つ折り曲げ部または折り曲げ部で折り曲げられると、その第１主面（表主面）に搭載される半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドと、前記積層体の同一機能の配線をショートカットするショートカット用配線接続部を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記四つ折り曲げ部または折り曲げ部で折り曲げて前記可撓性配線基板の第１主面（表主面）に搭載された半導体チップを重ね合わされて積層する工程と、前記半導体チップが重ね合わされた積層体間に熱伝導性接着テープと熱吸収パッドで冷却路を形成する工程と、前記積層体の同一機能の配線のショートカット用配線同志を電気的に接続する工程とを備えた半導体装置の製造方法である。

【００２０】第１６の発明は、四つ折り曲げ部または折り曲げ部を有し、四つ折り曲げ部で折り曲げられると、その第１主面（表主面）に搭載される隣合せの半導体チップが重ね合わされる位置に少なくとも１組の半導体チップ積層体に対応する半導体チップ搭載用ランドを有し、前記可撓性配線基板の第２主面（裏主面）に設けられた前記積層体の同一機能の配線の共通端子を有する可撓性配線基板を用意する工程と、前記複数組の半導体チップ搭載用ランドと半導体チップの外部電極（パッド）とを電気的に接続し、該電気的接続部を封止材で封止して可撓性配線基板上に半導体チップを搭載する工程と、前記可撓性配線基板の前記折り曲げ部で折り曲げて前記可撓性配線基板の第１主面（表主面）に搭載された隣合せの半導体チップを重ね合わされて積層する工程と、前記半導体チップが重ね合わされた積層体間に熱伝導性接着テープと熱吸収パッドで冷却路を形成する工程と、前記積層体の同一機能の配線をショートカットするショートカット用配線を電気的に接続する工程と、前記積層体の同一機能の配線の共通端子と実装基板のランドとを電気的に接続する工程とを備えた半導体装置の製造方法である。

【００２１】

【発明の実施の形態】以下、本発明について、図面を参照して実施の形態（実施例）とともに詳細に説明する。なお、実施例を説明するための全図において、同一機能を有するものは同一符号を付け、その繰り返しの説明は省略する。

【００２２】（実施例１）図１は本発明の実施例１の半導体装置の概要構成を示す正面図であり、図２は本実施例１の半導体装置を実装基板に実装した正面図である。本実施例１の半導体装置は、図１に示すように、折り曲げ部を有する可撓性配線基板２の表主面（第１主面）に所定の間隔で複数の半導体チップ（ＩＣチップ）１が搭載され、前記可撓性配線基板２の前記折り曲げ部で折り曲げられて、前記可撓性配線基板２の表主面に搭載された隣合せの半導体チップ１が背中合わせに重ね合わされ、接着材（又は接着テープ）２Ｂで固定される。さらに、前記可撓性配線基板２の前記折り曲げ部２Ａで折り曲げられて、次の１組の積層体が積層される。このようにして複数組の積層体が構成される。該複数組の積層体の前記各積層体の同一機能の配線をショートカット配線

基板８で電気的に接続して前記可撓性配線基板２の配線長をショートカットする。前記可撓性配線基板２の厚さは、例えば、７５μｍ、Ｃｕ配線の厚さは３５μｍである。

【００２３】図２に示すように、本実施例１の半導体装置１００は、前記可撓性配線基板２の裏主面（第２主面）に設けられている実装用半田ボール端子（配線の共通端子）７と実装基板９の半導体装置実装用ランド９Ａとを電気的に接続して前記実装基板９に実装される。

【００２４】次に、本実施例１の半導体装置の製造方法について説明する。図３は前記可撓性配線基板２の配線構成を示す表平面図、図４は前記可撓性配線基板２の配線構成を示す裏平面図、図５は前記可撓性配線基板２上に半導体チップ１を搭載した状態を示す全体平面図、図６は図５の側面図、図７は１個の半導体チップ１を前記可撓性配線基板２上に搭載した状態を示す断面図、図８は前記ショートカット配線基板８Ａ，８Ｂの一方の配線基板８Ａと他方の配線基板８Ｂの配線構成を示す平面図、図９は前記ショートカット配線基板８Ａ，８Ｂの一方の配線基板８Ａを前記可撓性配線基板２の配線に接続した状態を示す図である。

【００２５】図３～図９において、１は半導体チップ（ＩＣチップ）、１Ａは半導体チップの外部電極（パッド上のＡｕバンプ）、２は可撓性配線基板（フレキシブル配線基板）、２Ａは折り曲げ部、３は配線、４はショートカット配線接続用Ａｕバンプ、５はビア、６は半導体チップ搭載用ランド、７は実装用半田ボール端子（共通配線外部端子）、８Ａ，８Ｂはショートカット配線基板、８Ａ１，８Ｂ１はショートカット配線ランド、９は実装基板、９Ａは実装基板上の半導体装置実装用ランド、１０は封止材、１１はフレキシブル基板テープ、１２は絶縁膜（保護膜）である。

【００２６】まず、図３に示すような可撓性配線基板（フレキシブル配線基板）２を製造する。前記可撓性配線基板（フレキシブル配線基板）２の製造は、図３に示すように、フレキシブル基板テープ１１に配線を形成し、その上に絶縁膜（保護膜）１２を被覆する。この配線が形成されたフレキシブル基板テープ１１の表主面に、半導体チップ１の同一機能の半導体チップ搭載用ランド６を接続する配線３、半導体チップ１の同一機能の半導体チップ搭載用ランド６を接続するショートカット配線接続用Ａｕバンプ４、前記配線３を通すビア５、及び半導体チップ搭載用ランド６をそれぞれ所定位置に形成する。前記フレキシブル基板テープ１１の裏主面には、図４に示すように、半導体チップ１の同一機能の半導体チップ搭載用ランド６を接続する配線３及びショートカット配線接続用Ａｕバンプ４並びに実装用半田ボール端子（共通配線外部端子）７を形成する。

【００２７】本実施例１の半導体装置の製造方法は、前記図３に示すような可撓性配線基板（フレキシブル配線基板）２を用意する。次に、図５及び図６に示すように、前記可撓性配線基板２の表主面に所定の間隔で形成された半導体チップ搭載用ランド６上に、半導体チップの外部電極（パッド上のＡｕバンプ）１Ａを電気的に接続して複数の半導体チップ（ＩＣチップ）１を搭載する。すなわち、半導体チップ（ＩＣチップ）１は、図７に示すように、半導体チップ搭載用ランド６と外部電極（パッド上のＡｕバンプ）１Ａとを電気的に接続し、その接続部を封止材（封止樹脂）１０で封止する。

【００２８】前記複数の半導体チップ１が搭載された前記可撓性配線基板２の前記折り曲げ部２Ａで、図６に示す矢印方向に折り曲げられて、前記可撓性配線基板２の表主面に搭載された隣合せの半導体チップ１が背中合わせに重ね合せ、接着材（又は接着テープ）２Ｂで固定する。さらに、前記可撓性配線基板２の前記折り曲げ部２Ａで折り曲げて、ショートカット配線接続用Ａｕバンプ４とショートカット配線接続用ランド４Ａとを接続し、次の１組の積層体を積層する。このようにして複数組の積層体を構成する。

【００２９】前記複数組の積層体の前記各積層体の同一機能の配線を、図９に示すように、まず、図８（ａ）に示すショートカット配線基板８Ａで左側の積層体の同一機能の配線のショートカット配線接続用Ａｕバンプ４を電気的に接続し、次に、図８（ｂ）に示すショートカット配線基板８Ｂのショートカット配線ランド８Ｂ１と右側の積層体の同一機能の配線のショートカット配線接続用Ａｕバンプ４を電気的に接続する。これにより前記可撓性配線基板２の配線長をショートカットすることができる。このようにして、図１に示すような半導体装置１００を完成する。前記半導体装置１００は、図２に示すように、前記積層体の同一機能の配線の共通端子である実装用半田ボール端子（配線の共通端子）７と実装基板９上の半導体装置実装用ランド９Ａとを電気的に接続する。

【００３０】以上説明したように本実施例１によれば、折り曲げ可能な可撓性配線基板２を用い、前記各積層体の同一機能の配線をショートカット配線基板８Ａ、８Ｂで電気的に接続して、前記可撓性配線基板２の配線長をショートカットするので、配線長による信号遅延を防止することができる。また、配線基板を折り畳んで立体構造（三次元）にした半導体装置において、前記各積層体の同一機能の配線をショートカット配線基板８Ａ，８Ｂにより積層体内部の熱の放熱効率を向上させることができる。また、実装用半田ボール端子部以外の基板の両面にＩＣチップを両面実装することも可能である。

【００３１】（実施例２）図１０は本発明の実施例２の半導体装置の概要構成を示す正面図であり、図１１は本実施例２の半導体装置を実装基板に実装した正面図である。本実施例２の半導体装置は、前記実施例１のショートカット配線基板８Ａ，８Ｂを省略した実施例である

すなわち、図１０に示すように、折り曲げ部２Ａを有する可撓性配線基板２の表主面に所定の間隔で複数の半導体チップ（ＩＣチップ）１が搭載され、前記可撓性配線基板２の前記折り曲げ部２Ａで折り曲げられて、前記可撓性配線基板２の表主面（第１主面）に搭載された隣合せの半導体チップ２が背中合わせに重ね合わされ、接着材（又は接着テープ）２Ｂで固定される。さらに、前記可撓性配線基板２の前記折り曲げ部２Ａで折り曲げられて、ショートカット配線接続用Ａｕバンプ４とショートカット配線接続用ランド４Ａとを接続し、次の１組の積層体が積層される。このようにして複数組の積層体が構成される。該複数組の積層体の前記各積層体の同一機能の配線のショートカット配線接続用ランド４Ａとショートカット配線接続用Ａｕバンプ４とを電気的に接続して前記可撓性配線基板２の配線長をショートカットする。

【００３２】図１１に示すように、本実施例２の半導体装置２００は、前記可撓性配線基板２の裏主面（第２主面）に設けられている実装用半田ボール端子（配線の共通端子）７と実装基板９の半導体装置実装用ランド９Ａとを電気的に接続して前記実装基板９に実装される。

【００３３】次に、本実施例２の半導体装置の製造方法について説明する。図１２は前記可撓性配線基板２の配線構成を示す表平面図、図１３は前記可撓性配線基板２の配線構成を示す裏平面図、図１４は前記可撓性配線基板２上に半導体チップ１を搭載した状態を示す全体平面図、図１５は図１４の側面図、図１６は１個の半導体チップ１を前記可撓性配線基板２の表主面に搭載した状態を示す断面図、図１７は前記半導体チップ１を搭載された可撓性配線基板２を折り曲げて前記半導体チップ１を積層する状態を示す図、図１８は前記可撓性配線基板２の折り曲げ部で折り曲げてショートカット用配線を接続した状態の拡大断面図である。

【００３４】図１０～図１８において、１は半導体チップ（ＩＣチップ）、１Ａは半導体チップの外部電極（パッド上のＡｕバンプ）、２は可撓性配線基板（フレキシブル配線基板）、２Ａは折り曲げ部、３は配線、４はショートカット配線接続用Ａｕバンプ、４Ａはショートカット配線接続用ランド、５はビア、６は半導体チップ搭載用ランド、７は実装用半田ボール端子（共通配線外部端子）、９は実装基板、９Ａは実装基板上の半導体装置実装用ランド、１０は封止材、１１はフレキシブル基板テープ、１２は絶縁膜（保護膜）である。

【００３５】まず、図１２に示すような可撓性配線基板（フレキシブル配線基板）２を製造する。前記可撓性配線基板（フレキシブル配線基板）２の製造は、図１２に示すように、フレキシブル基板テープ１１の表主面（第１主面）に配線を形成し、その上に絶縁膜（保護膜）１２を被覆する。この配線が形成されたフレキシブル基板テープ１１の表主面に、半導体チップ１の同一機能の半導体チップ搭載用ランド６を接続する配線３、半導体チップ１の同一機能の半導体チップ搭載用ランド６を接続するショートカット配線接続用ランド４Ａとショートカット配線接続用Ａｕバンプ４、前記配線３を通すビア５、及び半導体チップ搭載用ランド６をそれぞれ所定位置に形成する。前記フレキシブル基板テープ１１の裏主面（第２主面）には、図１３に示すように、半導体チップ１の同一機能の半導体チップ搭載用ランド６を接続する配線３ショートカット配線接続用ランド４Ａ、及びショートカット配線接続用Ａｕバンプ４並びに実装用半田ボール端子７を形成する。

【００３６】本実施例２の半導体装置の製造方法は、前記図１２に示すような可撓性配線基板（フレキシブル配線基板）２を用意する。次に、図１４及び図１５に示すように、前記可撓性配線基板２の表主面に所定の間隔で形成された半導体チップ搭載用ランド６上に複数の半導体チップ（ＩＣチップ）１を搭載する。半導体チップ（ＩＣチップ）１は、図１６に示すように、半導体チップ搭載用ランド６と外部電極（パッド上のＡｕバンプ）１Ａとを電気的に接続し、その接続部を封止材（封止樹脂）１０で封止する。

【００３７】前記複数の半導体チップ１が搭載された前記可撓性配線基板２の前記折り曲げ部２Ａで折り曲げられて、図１７に示すように、前記可撓性配線基板２の表主面に搭載された隣合せの半導体チップ２が背中合わせに重ね合せ、接着材（又は接着テープ）２Ｂで固定する。さらに、図１７に示すように、前記可撓性配線基板２の前記折り曲げ部２Ａで折り曲げて、ショートカット配線接続用Ａｕバンプ４とショートカット配線接続用ランド４Ａとを接続し、次の１組の積層体を積層する。このようにして複数組の積層体を構成する。

【００３８】前記折り曲げ部の構成を図１８（ａ）、（ｂ）に示す。前記複数組の積層体の前記各積層体の同一機能の配線をショートカット配線部２Ｃで電気的に接続して前記可撓性配線基板２の配線長をショートカットして、図１０に示すような半導体装置２００を完成する。この半導体装置２００は、図１１に示すように、前記積層体の同一機能の配線の共通配線外部端子である実装用半田ボール端子７と実装基板９上の半導体装置実装用ランド９Ａとを電気的に接続する。

【００３９】以上説明したように、本実施例２によれば、折り曲げ可能な可撓性配線基板２を用い、前記各積層体の同一機能の配線をショートカット配線部で電気的に接続して、前記可撓性配線基板２の配線長をショートカットするので、配線長による信号遅延を防止することができる。また、配線基板を折り畳んで立体構造（三次元）にした半導体装置において、前記各積層体の同一機能の配線をショートカット配線部により積層体内部の熱の放熱効率を向上させることができる。また、実装用半田ボール端子部以外の基板の両面にＩＣチップを両面実装することも可能である。

【００４０】（実施例３）本発明の実施例３の半導体装置（３００ｏｒ４００）は、前記実施例２と同様に前記実施例１のショートカット配線基板８を省略した別の実施例である。前記実施例１、２と同様にして、図１９又は図２０に示すような折り畳み構造にしたもの（３００ｏｒ４００）である。この製造方法は、前記実施例１、２と同様にして製造することができる。

【００４１】（実施例４）図２１は本発明の実施例４の半導体装置の概要構成を示す平面図、横断面図及び縦断面図であり、図２２は本実施例４の半導体装置を実装基板に実装した横断面図である。本実施例４の半導体装置は、図２１に示すように、四つ折り曲げ部２Ａを有するフレキシブル配線基板６３の表主面（第１主面）に所定の間隔で複数の半導体チップ（ＩＣメモリチップ）１が搭載され、前記フレキシブル配線基板６３の前記折り曲げ部で二つ折りに曲げられて、前記フレキシブル配線基板６３の表主面に搭載された隣合せの半導体チップ１が背中合わせに重ね合わされ、接着材（又は接着テープ）で固定される。さらに、前記フレキシブル配線基板６３の前記四つ折り曲げ部で四つ折りに曲げられて、次の１組の積層体が積層される。このようにして複数組の積層体が構成される。該複数組の積層体の前記各積層体の同一機能の配線のショートカット配線接続用ランド６１とショートカット配線接続用半田ボール端子６２とを電気的に接続して前記フレキシブル配線基板６３の配線長をショートカットされる。前記フレキシブル配線基板６３の中央部には折り曲げストレス緩和用抜き穴２６が設けられている。

【００４２】本実施例４の半導体装置５００は、図２２に示すように、前記フレキシブル配線基板６３の裏主面（第２主面）に設けられている実装用半田ボール端子（配線の共通端子）７と実装基板９の半導体装置実装用ランド９Ａとを電気的に接続されて前記実装基板９に実装される。

【００４３】次に、本実施例４の半導体装置の製造方法について説明する。図２３は前記フレキシブル配線基板６３の配線構成を示す表平面図、図２４は前記フレキシブル配線基板６３の配線構成を示す裏平面図、図２５は前記フレキシブル配線基板６３上に半導体チップ１を搭載した状態を示す全体平面図、図２６は図２５の側面図、図２７は１個の半導体チップ１を前記フレキシブル配線基板６３上に搭載した状態を示す断面図、図２８は前記半導体チップ１を搭載されたフレキシブル配線基板６３を二つ折りに曲げた平面図、横断面図、及び縦断面図、図２９は前記半導体チップ１を搭載されたフレキシブル配線基板６３を四つ折りに曲げた平面図である。

【００４４】図２１～図２９において、１は半導体チップ（ＩＣチップ）、１Ａは半導体チップの外部電極（パッド上のＡｕバンプ）、３は配線、６は半導体チップ搭載用ランド、７は実装用半田ボール端子（共通配線外部端子）、９は実装基板、９Ａは実装基板上の半導体装置実装用ランド、１０は封止材、１２は絶縁膜（保護膜）、５はビア、１７は微小（ビルドアップ）ビア、２６は折曲げストレス緩和用抜き穴、６１はショートカット接続配線用ランド、６２はショートカット配線用半田ボール端子、６３はポリイミドテープに配線を形成したフレキシブル配線基板（可撓性配線基板）である。

【００４５】まず、図２１に示すようなフレキシブル配線基板６３を製造する。前記フレキシブル配線基板６３の製造は、図２３及図２４に示すように、フレキシブル配線基板６３の配線を形成し、その上に絶縁膜（保護膜）を被覆する。このフレキシブル配線基板６３の表主面（第１主面）に、半導体チップ１の同一機能の半導体チップ搭載用ランドを接続する配線３、半導体チップ１の同一機能の半導体チップ搭載用ランドを接続するショートカット配線接続用ランド６１、ショートカット配線用半田ボール端子６２バンプ、及び半導体チップ搭載用ランド６をそれぞれ所定位置に形成する。前記フレキシブル配線基板６３の裏主面（第２主面）には、図２４に示すように、半導体チップ１の同一機能の半導体チップ搭載用ランドを接続する配線３、ショートカット配線接続用ランド６１、及びショートカット配線接続用Ａｕバンプ６２、並びに実装用半田ボール端子７を形成する。

【００４６】本実施例４の半導体装置の製造方法は、前記図２３及び図２４に示すようなフレキシブル配線基板６３を用意する。次に、図２５及び図２６に示すように、前記フレキシブル配線基板６３の表主面に所定の間隔で形成された半導体チップ搭載用ランド上に複数の半導体チップ（ＩＣチップ）１を搭載する。半導体チップ（ＩＣチップ）１は、図２７に示すように、半導体チップ搭載用ランドと外部電極（パッド上のＡｕバンプ）１Ａとを電気的に接続し、その接続部を封止材（封止樹脂）で封止する。

【００４７】また、多層配線を必要とされる場合は、前記図２７に示すように、フレキシブル配線基板６３にビルドアップ方式等を部分的に使用することで、高度な配線の可能な多層配線部（図左端より中央部右の最も薄い部分手前まで及び右端の厚くなっている部分）と片面あるいは両面の単層配線で折り曲げ可能な部位（前記多層配線部に挟まれた最も薄い部分）の共存するフレキシブル配線基板６３が作成可能となる。

【００４８】前記複数の半導体チップ１が搭載された前記フレキシブル配線基板６３の前記折り曲げ部２Ａで二つ折りに曲げられて、図２８に示すように、前記フレキシブル配線基板６３の表主面に搭載された隣合せの半導体チップ１が背中合わせに重ね合せ、接着材（又は接着テープ）で固定する。さらに、図２９に示すように、前記フレキシブル配線基板６３の前記折り曲げ部２Ａで四つ折りに曲げて、次の１組の積層体を積層する。このようにして前記図２１に示すような半導体チップ１が背中

合わせに重ね合せた複数組の積層体を構成する。前記複数組の積層体の前記各積層体の同一機能の配線をショートカットさせる短絡電極で電気的に接続して前記フレキシブル配線基板６３の配線長をショートカットする。

【００４９】本実施例４の半導体装置５００は、図２２に示すように、前記フレキシブル配線基板６３の裏主面（第２主面）に設けられている共通端子である実装用外部電極７と実装基板９の半導体装置実装用ランド９Ａとを電気的に接続して前記実装基板９に実装される。なお、折曲げストレスが大きくない場合は折り曲げストレス緩和用抜き穴２６を設けなくてもよい。また、実装用半田ボール端子部以外の基板の両面にＩＣチップを両面実装することも可能である。

【００５０】（実施例５）図３０は本発明の実施例５の半導体装置の吸熱パッドをパッケージ内に収納した状態の概要構成を示す断面図、図３１は図３０の吸熱パッドをパッケージ内に収納した状態の概要構成を示す平面図、図３２は図３０の吸熱パッドによる冷却機構の概要構成を示す模式図である。

【００５１】図３０～図３２において、１は半導体チップ（ＩＣチップ）、１Ａは半導体チップの外部電極（パッド上のＡｕバンプ）、７は実装用半田ボール端子（共通配線外部端子）、２６は折曲げストレス緩和用抜き穴、６１はショートカット配線接続用ランド、６２はショートカット配線接続用半田ボール端子、６３はポリイミドテープ（フレキシブル基板）、６４は吸熱パット、６５はパイプ、６６は水路、６７はファン、６８は放熱部（ラジエター）、６９は放熱フイン、７０は冷却液循環ポンプ、７１は折り畳み積層パッケージ、７２は熱伝導接着テープである。

【００５２】本発明の実施例５の半導体装置は、前記実施例のような蛇腹折りや二つ折り、三つ折りの以外に十字折りのある折曲げ積層化ができる例であり、図３０及び図３１に示すように、フレキシブル配線基板６３（可撓性配線基板）を四つ折りにして半導体チップ１を積層するものである。そして、十字に折られてストレスの集中するフレキシブル配線基板６３の中央部に折り曲げストレス緩和用抜き穴２６が設けられたものである。

【００５３】すなわち、四つ折り曲げ部と中央部に折り曲げストレス緩和用抜き穴２６を有し、複数の半導体チップ１が表面に所定の間隔で搭載可能なフレキシブル配線基板６３と、該フレキシブル配線基板６３の前記二つ折り曲部で折り曲げられて前記フレキシブル配線基板６３の表面に搭載された半導体チップ１が背中合わせで重ね合わされた複数組の積層体とを備えた半導体装置であって、前記フレキシブル配線基板６３の表主面に所定位置に複数の半導体チップ（ＩＣメモリチップ）１が搭載され、前記可撓性配線基板２の前記折り曲部２Ａで四つ折りに曲げられて、前記フレキシブル配線基板６３の表主面に搭載された半導体チップ１が背中合わせに重ね合わされ、接着材（又は接着テープ）２Ｂで固定される。さらに、前記フレキシブル配線基板６３の前記折り曲部２Ａで四つ折り曲げられて、次の１組の積層体が積層されている。このようにして複数組の積層体が構成されている。

【００５４】前記フレキシブル配線基板６３に用いられる可撓性テープ基材の厚さは、例えば、７５μｍ、Ｃｕ配線の厚さは３５μｍである。該複数組の積層体の前記各積層体の同一機能の配線をショートカットさせる短絡電極で電気的に接続して前記フレキシブル配線基板６３の配線長をショートカットする。

【００５５】また、図３０及び図３１に示すように、前記半導体チップが重ね合わされた積層体間に吸熱パット（冷却路）６４が設けられている。前記吸熱パット（冷却路）６４は、図３０及び図３１に示すように、水路６６が形成されたものである。この吸熱パット（冷却路）６４は、折り畳み積層パッケージ７１の前記半導体チップが重ね合わされた積層体間に、熱伝導接着テープ７２により固定されている。

【００５６】また、前記吸熱パッド６４は、ＩＣパッケージ等に使用される絶縁セラミックス等の内部に水路６６を持つものである。前記水路６６はパイプ６５を通じて放熱部６８につながっており、内部は水等の液体を充填してある。吸熱パッド６４の取り付けには熱伝導接着テープ７２を使用するが、より高性能を狙ってシリコングリス＋接合材を使用してもよい。冷却液循環ポンプ７０で強制的に内部の液体を循環させ、吸熱パッド６４で吸収した熱を循環する液体を媒介してパイプ６５を通して放熱部６８に送りファン６７で強制冷却する。放熱部６８で冷された液体はパイプ６５を通して再び吸熱パッド６４に送られる。他にもヒートパイプや放熱板等を挟み込んだり、ヒートシンクを取り付けることもよい。

【００５７】また、多層配線を必要とされる場合は、前述した図２７に示すようにして、フレキシブル配線基板６３にビルドアップ方式等を部分的に使用することで、高度な配線の可能な多層配線部（図左端より中央部右の最も薄い部分手前まで及び右端の厚くなっている部分）と片面あるいは両面の単層配線で折り曲げ可能な部位（前記多層配線部に挟まれた最も薄い部分）の共存するフレキシブル配線基板６３を作成する。

【００５８】前記ビルドアップ多層配線部は、ポリイミドテープ（フレキシブル基板）６３の上に銅等の導電性物質で配線３を作り、絶縁感光性樹脂１８を積み、露光により微小（ビルドアップ）ビア１７を開けながら他の部分を硬化させ絶縁層として上に銅等の導電性物質で配線３を作りこんでいくため、単層配線で折り曲げ可能な部位も微小（ビルドアップ）ビア１７と同様の方法で製造可能となる。

【００５９】実施例１～５では、Ａｕバンプによるベアチップ実装による製造方法で説明しているが、他にワイ

ヤーボンデイングやビームリード等他の製造方法も可能なのは言うまでもない。また、前記実施例では半導体装置及びその製造方法について説明したが、本発明は、半導体モジュール及びその製造方法にも適用できることは前記説明から明らかである。

【００６０】以上、本発明を、前記実施例に基づき具体的に説明したが、本発明は、前記実施例に限定されるものではなく、その要旨を逸脱しない範囲において種々変更可能であることは勿論である。

【００６１】

【発明の効果】本願において開示される発明によって得られる効果を簡単に説明すれば、以下のとおりである。本願発明によれば、可撓性配線基板を折り畳んで立体構造（三次元）にした半導体装置もしくは半導体モジュールにおいて、配線をショートカットさせる短絡電極で電気的に接続して配線長をショートカットするので、配線長による信号遅延を防止することができる。また、前記半導体チップが重ね合わされた積層体間に吸熱パット（冷却路）が設けられているので、放熱効率を向上することができる。

【図面の簡単な説明】

【図１】本発明の実施例１の半導体装置の概要構成を示す正面図である。

【図２】本実施例１の半導体装置を実装基板に実装した正面図である。

【図３】本実施例１の可撓性配線基板の配線構成を示す表平面図である。

【図４】本実施例１の可撓性配線基板の配線構成を示す裏平面図である。

【図５】本実施例１の可撓性配線基板上に半導体チップを搭載した状態を示す全体平面図である。

【図６】図５の側面図である。

【図７】本実施例１の１個の半導体チップを可撓性配線基板上に搭載した状態を示す断面図である。

【図８】本実施例１のショートカット配線基板の一方の配線基板と他方の配線基板の配線構成を示す平面図である。

【図９】本実施例１のショートカット配線基板の一方の配線基板を可撓性配線基板の配線に接続した状態を示す図である。

【図１０】本発明の実施例２の半導体装置の概要構成を示す正面図である。

【図１１】本実施例２の半導体装置を実装基板に実装した正面図である

【図１２】本実施例２の可撓性配線基板２の配線構成を示す表平面図である。

【図１３】本実施例２の可撓性配線基板の配線構成を示す裏平面図である。

【図１４】本実施例２の可撓性配線基板上に半導体チップを搭載した状態を示す全体平面図である。

【図１５】図１４の側面図である。

【図１６】本実施例２の１個の半導体チップ可撓性配線基板上に搭載した状態を示す断面図である。

【図１７】本実施例２の半導体チップを搭載された可撓性配線基板を折り曲げて半導体チップを積層する状態を示す図である。

【図１８】本実施例２の可撓性配線基板の折り曲げ部で折り曲げてショートカット用配線を接続した状態の拡大断面図である。

【図１９】本発明の実施例３の半導体装置の概要構成を示す正面図、平面図及び側面図である。

【図２０】本発明の実施例３の半導体装置の概要構成を示す正面図である。

【図２１】本発明の実施例４の半導体装置の概要構成を示す平面図、横断面図及び縦断面図である。

【図２２】本実施例４の半導体装置を実装基板に実装した横断面図である。

【図２３】本実施例４の可撓性配線基板の配線構成を示す表平面図である。

【図２４】本実施例４の可撓性配線基板の配線構成を示す裏平面図である。

【図２５】本実施例４の可撓性配線基板上に半導体チップを搭載した状態を示す全体平面図である。

【図２６】図２５の側面図である。

【図２７】本実施例４の１個の半導体チップを前記可撓性配線基板上に搭載した状態を示す断面図（多層配線使用時のもの）である。

【図２８】本実施例４の半導体チップを搭載された可撓性配線基板を二つ折りに曲げた平面図、横断面図、及び縦断面図である。

【図２９】本実施例４の半導体チップを搭載された可撓性配線基板を四つ折りに曲げた平面図である。

【図３０】本発明の実施例５の半導体装置の吸熱パッドをパッケージ内に収納した状態の概要構成を示す断面図である。

【図３１】本実施例５の吸熱パッドをパッケージ内に収納した状態の概要構成を示す平面図である。

【図３２】本実施例５の吸熱パッドによる冷却機構の概要構成を示す模式図である。

【符号の説明】

１…半導体チップ（ＩＣチップ）　１Ａ…半導体チップの外部電極

２…可撓性配線基板　２Ａ…折り曲部

２Ｂ…半導体チップ接着剤　２Ｃ…ショートカット配線接続部

３…配線　４…ショートカット配線接続用Ａｕバンプ

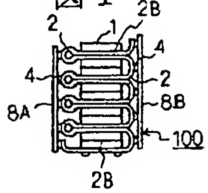
４Ａ…ショートカット配線接続用ランド

５…ビア　６…半導体チップ搭載用ランド

７…実装用半田ボール端子
８Ａ，８Ｂ…ショートカット配線基板
９…実装基板
９Ａ…半導体装置実装用ランド
１０…封止材
１１…フレキシブル基板テープ
１２…絶縁膜（保護膜）
１７…微小（ビルドアップ）ビア
１８…絶縁感光性樹脂
２２…接着テープ
２３…半田
２６…折曲げストレス緩和抜き穴
６１…ショートカット配線接続用ランド
６２…ショートカット配線用半田ボール端子
６３…フレキシブル配線基板
６４…吸熱パット
６５…パイプ
６６…水路
６７…ファン
６８…放熱部（ラジエター）
６９…放熱フイン
７０…冷却液循環ポンプ
７１…折り畳み積層パッケージ
７２…熱伝導接着テープ

【図１】

図１

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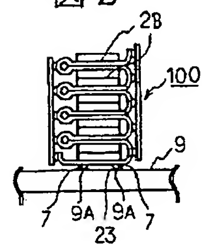


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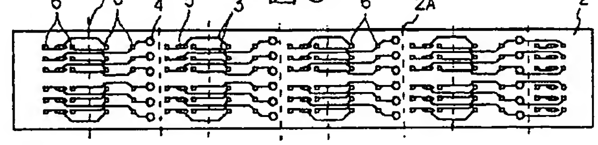


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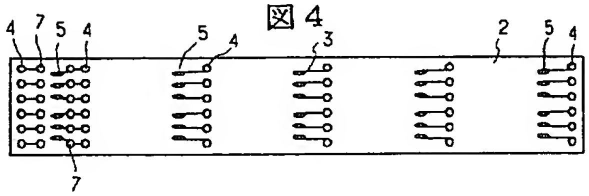


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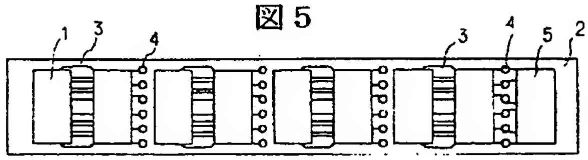


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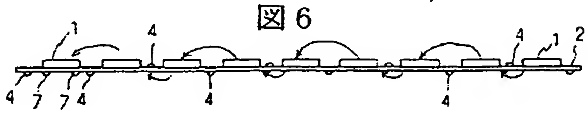


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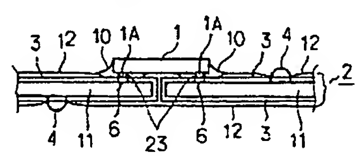


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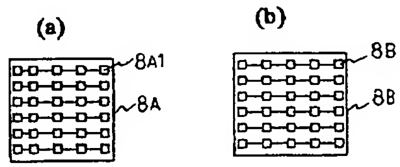


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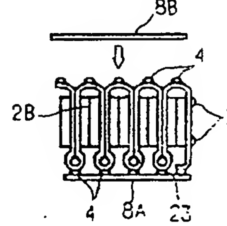


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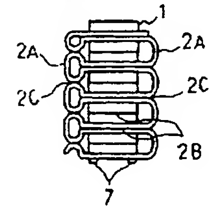

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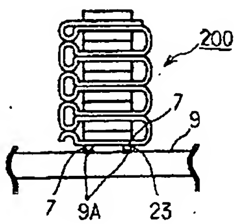


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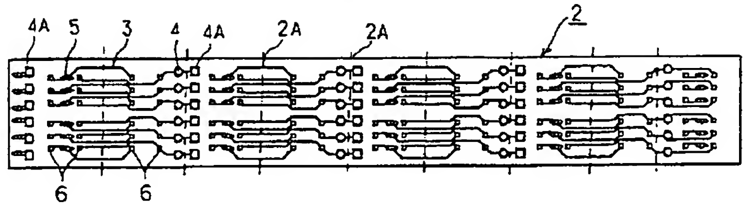


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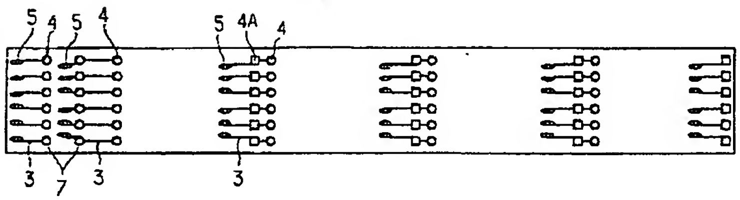


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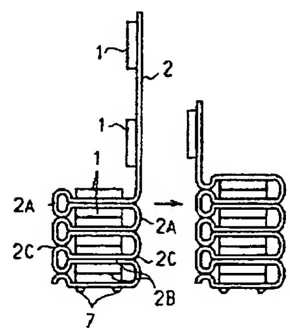


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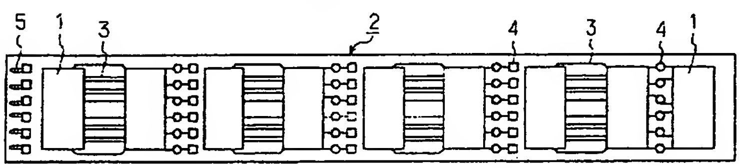


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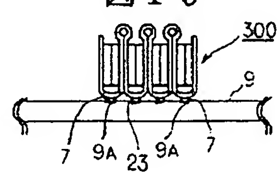


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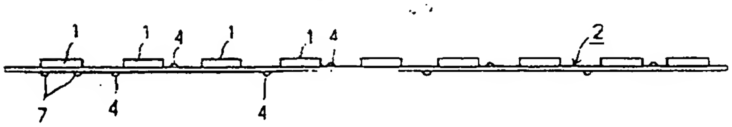


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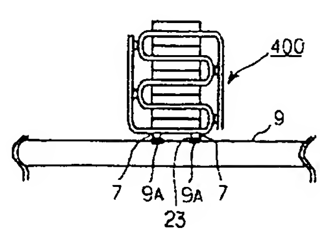

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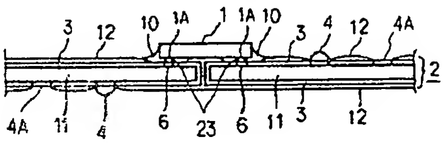


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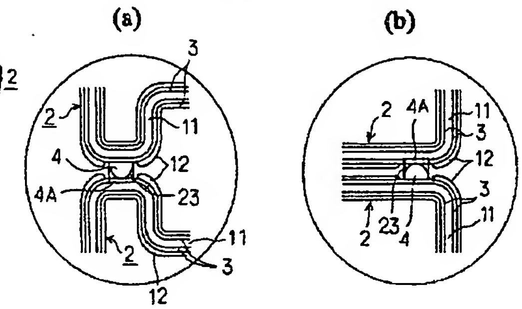


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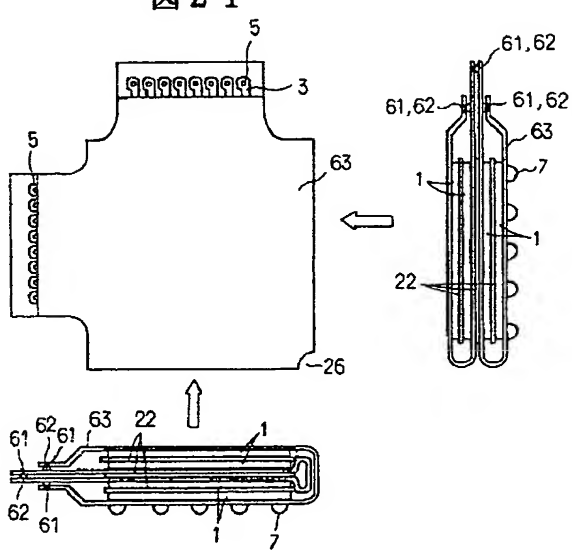


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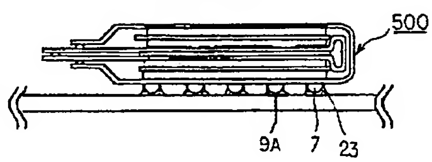


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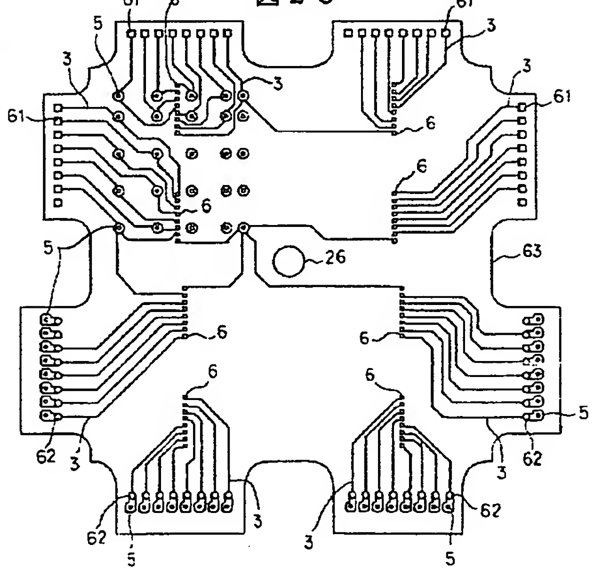


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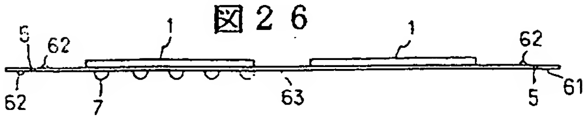

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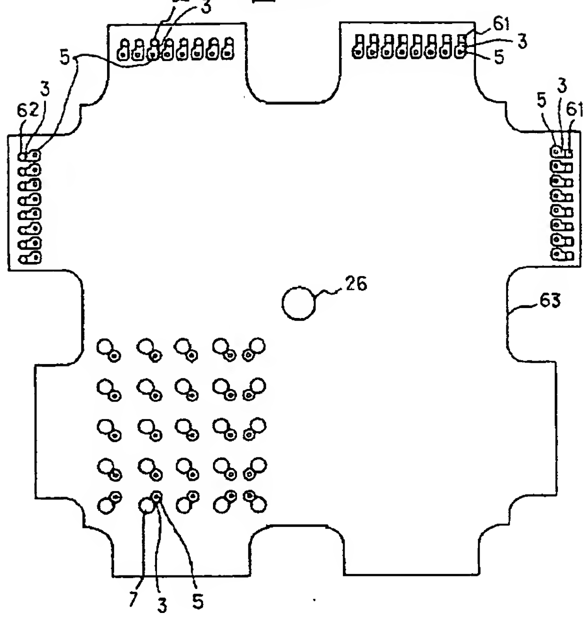


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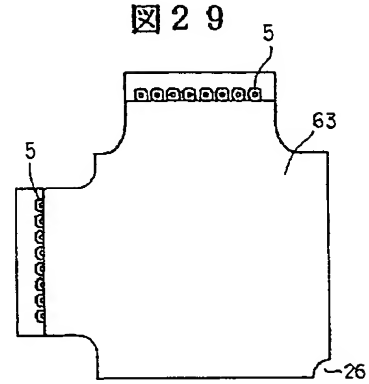


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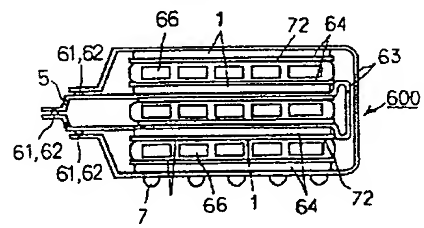


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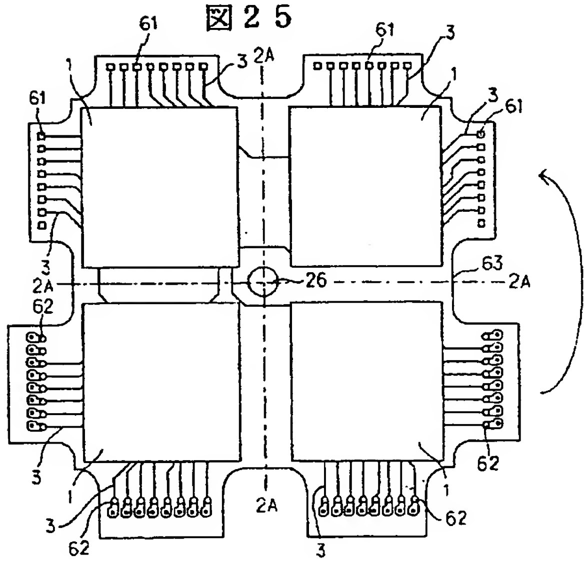


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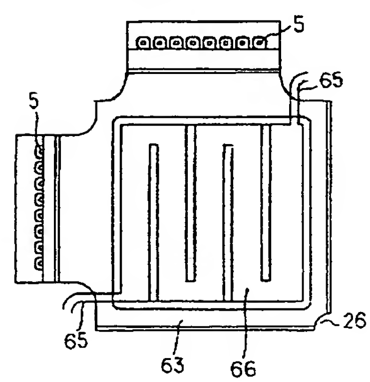

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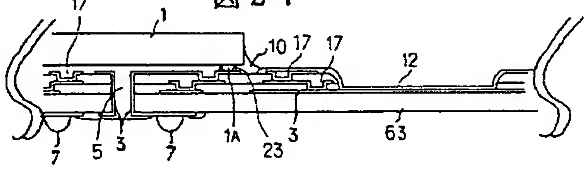


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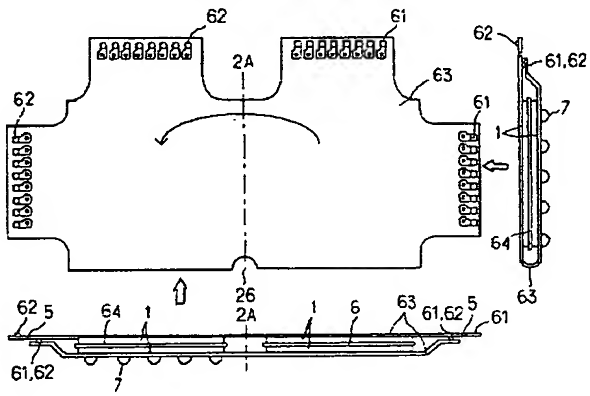


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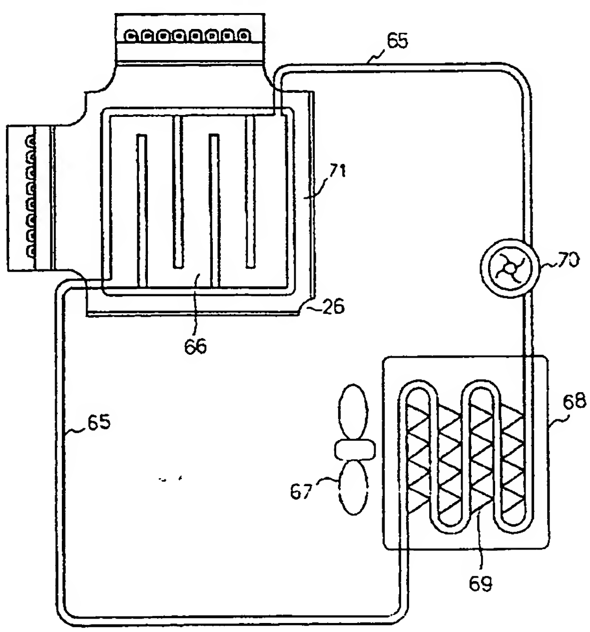

フロントページの続き

| (51)Int.Cl.7 | | 識別記号 | FI | | テーマコード(参考) |
|---|---|---|---|---|---|
| H01L | 25/07 | | H01L | 25/08 | Z |
| | 25/18 | | | 23/46 | Z |
| H05K | 1/02 | | | | C |
| | 1/14 | | | | |
| | 1/18 | | | | |

Fターム(参考) 5E336 AA04 AA16 BB02 BB05 BB12 BC21 CC31 CC55 DD16 DD18 EE07 GG03 GG11
5E338 AA02 AA12 BB13 BB25 BB51 BB54 CC01 EE02 EE13 EE14 EE23
5E344 BB02 BB03 BB04 CC25 DD16 EE02 EE06 EE30
5F036 AA01 BB21 BB35 BB43 BC05
5F044 MM16 MM50 NN02 RR03

JAPANESE PATENT OFFICE

PATENT JOURNAL (A)

KOKAI PATENT APPLICATION NO. P2003-347503A

| | | |
|---|---|---|
| Int. Cl.$^{7}$: | H 01 L | 25/065 |
| | | 21/60 |
| | | 23/467 |
| | | 23/473 |
| | H 01 L | 25/07 |
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| | H 05 K | 1/02 |
| | | 1/14 |
| | | 1/18 |
| | H 01 L | 25/08 |
| | | 23/46 |

| | |
|---|---|
| Filing No.: | P2002-156537 |
| Filing Date: | May 30, 2002 |
| Publication Date: | December 5, 2003 |
| No. of Claims: | 16 (Total of 17 pages; OL) |
| Examination Request: | Not filed |

# SEMICONDUCTOR DEVICE, METHOD OF MANUFACTURING SAME, AND SEMICONDUCTOR MOUNTING METHOD

| | |
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[There are no amendments to this patent.]

Abstract

Purpose

To prevent signal delay due to wiring length in a semiconductor device or semiconductor module having a three-dimensional (3-dimensional) structure by folding up a flexible wiring board. To increase the heat dissipation efficiency.

Constitution

A type of semiconductor device or semiconductor module characterized by the following facts: it has a flexible wiring board that has folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, and at least one set of laminates created by folding said flexible wiring board at said folding portions and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board; wirings having the same function of the laminates are electrically connected by shortcut wiring boards.

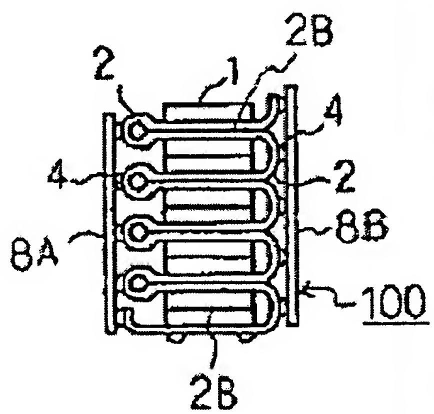



Figure 1

Claims

1. A type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding said flexible wiring board at said double folding portions and thereby superposing adjacent

semiconductor chips mounted on said first principal surface of said flexible wiring board, and shortcut wiring boards that electrically connect wirings having the same function of the laminates.

2. A type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding said flexible wiring board at said double folding portions and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board, shortcut wiring boards that electrically connect wirings having the same function of the laminates, common terminals for the wirings having the same function of said laminates arranged on the second principal surface of said flexible wiring board, and a means for forming an electrical connection between the common terminals and the wiring lands of the mounting substrate.

3. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions being sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; and a step in which wirings having the same function of said laminates are electrically connected with shortcut wiring boards.

4. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed, and which has common terminals for wirings having the same function of said laminates arranged on the second principal surface of said flexible wiring board; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that adjacent semiconductor chips

mounted on the first principal surface of said flexible wiring board are superposed and laminated; a step in which wirings having the same function of said laminates are electrically connected with shortcut wiring boards; and a step in which electrical connection is made between said common terminals and the wiring lands of the mounting substrate.

5. A type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding said flexible wiring board at said double folding portions and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board, and connecting portions that electrically connect wirings having the same function of the laminates to create wiring shortcuts.

6. A type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding said flexible wiring board at said double folding portions and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board, shortcut wiring boards that electrically connect wirings having the same function of the laminates, connecting portions that electrically connect wirings having the same function of said laminates to create wirings shortcuts, common terminals for the wirings having the same function of said laminates arranged on the second principal surface of said flexible wiring board, and a means that electrically connects the common terminals and the wiring lands of the mounting substrate.

7. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions, lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed and connecting portions for shortcut wirings that create shortcut for wirings having the same function of said laminates; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; and a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts.

8. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed, and that has common terminals for wirings having the same function of said laminates arranged on the second principal surface of said flexible wiring board; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; a step in which electrical connection of wirings having the same function of said laminates is made to create wiring shortcuts; and a step in which electrical connection is made between said common terminals having the same function of said laminates and the wiring lands of the mounting substrate.

9. A type of semiconductor device characterized by the fact that it has a flexible wiring board that has quarter folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding at said quarter folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board, and connecting portions that electrically connect wirings having the same function of the laminates to create wiring shortcuts.

10. A type of semiconductor device characterized by the fact that it has a flexible wiring board that has quarter folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding at said quarter folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board, shortcut wiring boards that electrically connect wirings having the same function of the laminates, connecting portions that electrically connect wirings having the same function of said laminates to create wiring shortcuts, common terminals for the wirings having the same function of said laminates arranged on the second principal surface of said flexible wiring board, and a means that electrically connects the common terminals and the wiring lands of the mounting substrate.

11. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter

folding portions, lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed when folding at said quarter folding portions, and connecting portions for the wirings having the same function of said laminates to create wiring shortcuts ; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said quarter folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; and a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts.

12. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed when folding at said quarter folding portions, and that has common terminals for wirings having the same function of said laminates arranged on the second principal surface of said flexible wiring board; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said quarter folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts; and a step in which electrical connection is made between said common terminals having the same function of said laminates and the lands of the mounting substrate.

13. A type of semiconductor device characterized by the following facts: it has a flexible wiring board that has quarter folding portions or double folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, at least one set of laminates created by folding at said quarter folding portions or double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board, and connecting portions that electrically connect wirings having the same function of the laminates to create wiring shortcuts; and a cooling path is provided between laminates with said superposed semiconductor chips.

14. A type of semiconductor device characterized by the following facts: it has a flexible wiring board that has quarter folding portions or double folding portions and allows plural semiconductor chips to be mounted on the first principal surface at prescribed intervals, and at least one set of laminates created by folding at said quarter folding portions or double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface of said flexible wiring board; the lands for shortcut wiring for wirings having the same function of said laminates are electrically connected, and electrical connection is made between the common terminals of the wirings having the same function of said laminates and the lands on the mounting substrate; in this semiconductor device, a cooling path is provided between the laminates with said superposed semiconductor chips; common terminals having the same function of said laminates are arranged on the second principal surface of said flexible wiring board; and electrical connection is made between said common terminals and the wiring lands of the mounting substrate.

15. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions or double folding portions, lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed when folding at said quarter folding portions and double folding portions, and connecting portions for wirings having the same function of said laminates to create wiring shortcuts; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said quarter folding portions or double folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; a step in which a cooling path is formed by means of thermoconductive adhesive tape and heat absorptive pads between said laminates with said superposed semiconductor chips; a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts.

16. A method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions or double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface are superposed when said quarter folding portions or double folding portions are folded, and which has common terminals for wirings having the same function of said laminates arranged on the second principal surface

of said flexible wiring board; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said [quarter folding portions or] double folding portions so that the adjacent semiconductor chips mounted on the first principal surface of said flexible wiring board are superposed and laminated; a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts; and a step in which electrical connection is made between said common terminals having the same function of said laminates and the lands of the mounting substrate.

Detailed explanation of the invention

[0001]

Technical field of the invention

The present invention pertains to a surface-mount type of semiconductor device or semiconductor module, and its manufacturing method. In particular, the present invention pertains to an effective technology in which plural semiconductor chips are mounted on a flexible wiring board (flexible wiring substrate) or a leadframe, and the adjacent semiconductor chips, that is, said mounted semiconductor chips, are attached back-to-back, and laminated.

[0002]

Prior art

As a semiconductor device of small size with a and high degree of integration, for example, Japanese Kokai Patent Application No. Hei 9[1997]-181215 proposed a type of semiconductor device characterized by the following facts: there is a package for assembling semiconductor chips in the stacked portions of a flexible wiring board (flexible wiring substrate), and there is also a package (sealed body) for mounting semiconductor chips on the side opposite the side where the external terminals for mounting semiconductor chips (lands for mounting semiconductor chips) on the flexible wiring board are positioned (see: Figures 22-24).

[0003]

Problems to be solved by the invention

After studying the aforementioned prior art, the present inventors have found the following problems. Although said prior art can realize a three-dimensional (3-D) structure with a small footprint and a high degree of integration, it has only a folded planar (two-dimensional) board as the substrate, so that the wiring length is the same as that in the conventional planar

board constitution. Consequently, the problem of signal delay due to the wiring length exists. Also, due to stacking of plural semiconductor chips (IC chips) in a narrow space, it is difficult for the heat generated in the package to dissipate, and defective operation may result. This is undesirable. Also, the solder ball terminals of the BGA (Ball Grid Array) cannot deform differently from the lead terminals, so that cracks or breakage may occur due to deformation or expansion of the mounting substrate.

[0004]

The purpose of the present invention is to provide a technology that can prevent signal delay due to wiring in the semiconductor device or semiconductor module in a three-dimensional (3-D) structure created by folding the board. Another purpose of the present invention is to provide a technology that can increase the heat dissipation efficiency of the semiconductor device or semiconductor module in a three-dimensional (3D) structure created by folding the board. The aforementioned and other purposes, as well as other novel features of the present invention, will be explained in the description and appended figures of the present specification.

[0005]

Means to solve the problems

In the following, a brief account will be presented for the inventions described in the present patent application. The first invention provides a type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, and shortcut wiring boards that electrically connect wirings having the same function of the laminates.

[0006]

The second invention provides a type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, shortcut wiring boards that electrically connect wirings having the same function of the

laminates, common terminals for the wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board, and a means for forming an electrical connection between the common terminals and the wiring lands of the mounting substrate.

[0007]

The third invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; and a step in which wirings having the same function of said laminates are electrically connected with shortcut wiring boards.

[0008]

The fourth invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed, and which has common terminals for wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board; a step in which electrical connection is made between the lands for mounting plural groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; a step in which wirings having the same function of said laminates

are electrically connected with shortcut wiring boards; and a step in which electrical connection is made between said common terminals and the wiring lands of the mounting substrate.

[0009]

The fifth invention provides a type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, and connecting portions that electrically connect wirings having the same function of the laminates to create wiring for shortcuts.

[0010]

The sixth invention provides a type of semiconductor device characterized by the fact that it has a flexible wiring board that has double folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, shortcut wiring boards that electrically connect wirings having the same function of the laminates, connecting portions that electrically connect wirings having the same function of said laminates to create wiring shortcuts, common terminals for the wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board, and a means that electrically connects the common terminals and the wiring lands of the mounting substrate.

[0011]

The seventh invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions, lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed and connecting portions of wirings for shortcuts that make shortcuts for the wirings having the same function of said laminates; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads)

of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; and a step in which electrical connection of wirings having the same function of said laminates is made to create wiring shortcuts.

[0012]

The eighth invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed, and which has common terminals for wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said double folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; a step in which electrical connection is made to create wiring shortcuts for the wirings having the same function of said laminates; and a step in which electrical connection is made between said common terminals having the same function of said laminates and the wiring lands of the mounting substrate.

[0013]

The ninth invention provides a type of semiconductor device characterized by the fact that it has a flexible wiring board that has quarter folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said quarter folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, and connecting portions that electrically connect wirings having the same function of the laminates to create wiring shortcuts.

[0014]

The tenth invention provides a type of semiconductor device characterized by the fact that it has a flexible wiring board that has quarter folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said quarter folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, shortcut wiring boards that electrically connect wirings having the same function of the laminates, connecting portions that electrically connect wirings having the same function of said laminates to create wiring shortcuts, common terminals of the wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board, and a means that electrically connects the common terminals and the wiring lands of the mounting substrate.

[0015]

The eleventh invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions, lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed when folding at said quarter folding portions, and connecting portions for wirings having the same function of said laminates to create wiring shortcuts; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said quarter folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; and a step in which electrical connection is made for wirings having the same function of said laminates to create shortcuts.

[0016]

The twelfth invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are

superposed when folding at said quarter folding portions, and which has common terminals of wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board; a step in which electrical connection is made between the lands for mounting groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said quarter folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts; and a step in which electrical connection is made between said common terminals having the same function of said laminates and the lands of the mounting substrate.

[0017]

The thirteenth invention provides a type of semiconductor device characterized by the following facts: it has a flexible wiring board that has quarter folding portions or double folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, at least one set of laminates created by folding at said quarter folding portions or double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board, and connecting portions that electrically connect wirings having the same function of the laminates to create wiring shortcuts; and a cooling path is provided between laminates with said superposed semiconductor chips.

[0018]

The fourteenth invention provides a type of semiconductor device characterized by the following facts: it has a flexible wiring board that has quarter folding portions or double folding portions and allows plural semiconductor chips to be mounted on the first principal surface (outer principal surface) at prescribed intervals, and at least one set of laminates created by folding at said quarter folding portions or double folding portions of said flexible wiring board and thereby superposing adjacent semiconductor chips mounted on said first principal surface (outer principal surface) of said flexible wiring board; the lands for shortcut wiring for wirings having the same function of said laminates are electrically connected, and electrical connection is made between the common terminals of the wirings having the same function of said laminates and the lands on the mounting substrate; in this semiconductor device, a cooling path is provided between the laminates with said superposed semiconductor chips; common terminals having the

same function of said laminates are arranged on the second principal surface (inner principal surface) of said flexible wiring board; and electrical connection is made between said common terminals and the wiring lands of the mounting substrate.

[0019]

The fifteenth invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions or double folding portions, lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed when folding at said quarter folding portions and double folding portions, and connecting portions for wirings having the same function of said laminates to create wiring shortcuts, is prepared; a step in which electrical connection is made between the lands for mounting plural groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips, the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible wiring board is folded at said quarter folding portions or double folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; a step in which a cooling path is formed by means of thermoconductive adhesive tape and heat absorptive pads between said laminates with said superposed semiconductor chips; a step in which electrical connection is made for wirings having the same function of said laminates to create the wiring shortcuts.

[0020]

The sixteenth invention provides a method of manufacturing semiconductor devices characterized by the fact that it has the following steps: a step in which a flexible wiring board is prepared that has quarter folding portions or double folding portions and lands for mounting semiconductor chips corresponding to at least one set of laminated semiconductor chips at the positions where the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) are superposed when said quarter folding portions or double folding portions are folded, and which has common terminals for wirings having the same function of said laminates arranged on the second principal surface (inner principal surface) of said flexible wiring board; a step in which electrical connection is made between the lands for mounting plural groups of semiconductor chips and the external electrodes (pads) of the semiconductor chips; a step in which the electrical connecting portions are sealed with a sealant, and the semiconductor chips are mounted on the flexible wiring board; a step in which said flexible

wiring board is folded at said [quarter folding portions or] double folding portions so that the adjacent semiconductor chips mounted on the first principal surface (outer principal surface) of said flexible wiring board are superposed and laminated; a step in which electrical connection is made for wirings having the same function of said laminates to create wiring shortcuts; and a step in which electrical connection is made between said common terminals having the same function of said laminates and the lands of the mounting substrate.

[0021]

Embodiments of the invention

In the following, an explanation will be given in detail regarding the embodiments (Application Examples) of the present invention, with reference to figures. The same part numbers are adopted throughout all of the figures used to illustrate the application examples, and they will not be explained repeatedly.

[0022]

Application Example 1

Figure 1 is a schematic front view illustrating the constitution of the semiconductor device in Application Example 1 of the present invention. Figure 2 is a front view illustrating the state in which the semiconductor device of Application Example 1 is mounted on a mounting substrate. As shown in Figure 1, in the semiconductor device of Application Example 1, plural semiconductor chips (IC chips) (1) are mounted at a prescribed interval on the outer principal surface (first principal surface) of flexible wiring board (2) having double folding portions. When said flexible wiring board (2) is folded at said double folding portions, adjacent semiconductor chips (1) mounted on the outer principal surface of said flexible wiring board (2) are superposed back-to-back, and adhesive (or adhesive tape) (2B) is used to fix them together. In addition, said flexible wiring board (2) is folded at said double folding portions (2A), and the next set of laminates are layered. In this way, plural sets of laminates are formed. Wiring with the same function of said laminates of said plural sets of laminates are electrically connected with shortcut wiring board (8) to reduce the wiring length of said flexible wiring board (2). Said flexible wiring board (2) has a thickness of, for example, 75 μm, and the Cu wiring has a thickness of, for example, 35 μm.

[0023]

As shown in Figure 2, for semiconductor device (100) of Application Example 1, electrical connection is made between mounting solder ball terminals (common wiring terminals) (7) provided on the inner principal surface (second principal surface) of said flexible wiring

board (2) and lands (9A) for semiconductor device mounting on mounting substrate (9), so that the semiconductor device is mounted on said mounting substrate (9).

[0024]

In the following, an explanation will be given regarding the method of manufacturing the semiconductor device in Application Example 1. Figure 3 is a outer plan view illustrating the wiring constitution of said flexible wiring board (2). Figure 4 is an inner plan view illustrating the wiring constitution of said flexible wiring board (2). Figure 5 is an overall plan view illustrating the state in which semiconductor chips (1) are mounted on said flexible wiring board (2). Figure 6 is a side view of Figure 5. Figure 7 is a cross section illustrating the state in which one semiconductor chip (1) is mounted on said flexible wiring board (2). Figure 8 is a plan view illustrating the wiring constitution of wiring board (8A) as one of said shortcut wiring boards (8A), (8B), and of the other wiring board (8B). Figure 9 is a diagram illustrating the state in which wiring board (8A), one of said shortcut wiring boards (8A), (8B), is connected to the wiring of said flexible wiring board (2).

[0025]

In Figures 3-9, (1) represents semiconductor chips (IC chips); (1A) represents the external electrodes of the semiconductor chips (Au bumps on the pads); (2) represents the flexible wiring board (flexible wiring substrate); (2A) represents the double folding portions; (3) represents wiring; (4) represents Au bumps for connection of shortcut wiring; (5) represents via; (6) represents lands for mounting the semiconductor chips; (7) represents solder ball terminals for mounting (external common wiring terminals); (8A), (8B) represent shortcut wiring boards; (8A1), (8B1) represent shortcut wiring lands; (9) represents a mounting substrate; (9A) represents lands for mounting of semiconductor device on the mounting substrate; (10) represents a sealant; (11) represents flexible board tape; and (12) represents an insulating film (protective film).

[0026]

First of all, flexible wiring board (flexible wiring substrate) (2) is manufactured as shown in Figure 3. As shown in Figure 3, when said flexible wiring board (flexible wiring substrate) (2) is manufactured, wiring is formed on flexible substrate tape (11), with insulating film (protective film) (12) covering it. On the outer principal surface of flexible substrate tape (11) with wiring formed on it as described, wiring (3) for connecting lands (6) for mounting semiconductor chips that have the same function on semiconductor chips (1), Au bumps (4) for shortcut wiring connection that connect lands (6) for mounting semiconductor chips that have the same function

on semiconductor chips (1), via (5) to let said wiring (3) pass through, and lands (6) for mounting semiconductor chips are formed at their respective positions. as shown in Figure 4, wiring (3) for connecting lands (6) for mounting semiconductor chips that have the same function on semiconductor chips (1), as well as Au bumps (4) for shortcut wiring connection and solder ball terminals (external common wiring terminals) (7) for mounting are formed on the inner principal surface of said flexible substrate tape (11).

[0027]

In the method of manufacturing the semiconductor device in Application Example 1, as shown in said Figure 3, a flexible wiring board (flexible wiring substrate) (2) is prepared. Then, as shown in Figures 5 and 6, external electrodes of the semiconductor chips (Au bumps on the pads) (1A) are electrically connected with lands (6), which are for mounting semiconductor chips and are formed at a prescribed interval on the outer principal surface of said flexible wiring board (2), in order to mount plural semiconductor chips (IC chips) (1). That is, as shown in Figure 7, for semiconductor chips (IC chips) (1), external electrodes (Au bumps on the pads) (1A) and lands (6) for mounting the semiconductor chips, are electrically connected, followed by sealing of the connection region with sealant (sealing resin) (10).

[0028]

As shown in Figure 6, said flexible wiring board (2) having said plural semiconductor chips (1) mounted on it is folded at said double folding portions (2A) in the direction indicated by arrows. As a result, adjacent semiconductor chips (1) mounted on the outer principal surface of said flexible wiring board (2) are superposed back-to-back, and they are fixed together with adhesive (or adhesive tape) (2B). Said flexible wiring board (2) is further folded at said double folding portions (2A), Au bumps (4) for shortcut wiring connection and lands (4A) for shortcut wiring connection are [electrically] connected, and the next sets of laminates are layered on. In this way, plural sets of laminates are formed.

[0029]

As shown in Figure 9, first of all, by means of shortcut wiring board (8A) shown in Figure 8(a), wirings having the same functions of said laminates of said plural sets of laminates are electrically connected to Au bumps (4) for shortcut wiring connection of wirings having the same function on the left side of the laminates. Then, shortcut wiring lands (8B1) of shortcut wiring board (8B) shown in Figure 8(b) are electrically connected to Au bumps (4) for shortcut wiring connection of wirings having the same function on the right side of the laminates. As a result, the wiring length of said flexible wiring board (2) can be reduced. As shown in Figure 1,

semiconductor device (100) is completed in this way. As shown in Figure 2, in said semiconductor device (100) electrical connection is performed between solder ball terminals for mounting (common wiring terminals) (7), as the common terminals for wirings of the laminates having the same function, and lands (9A) on mounting substrate (9) for semiconductor device assembly.

[0030]

As explained above, according to Application Example 1, flexible wiring board (2) that can be folded enables electrical connection to be performed for wirings of the laminates having the same function by means of shortcut wiring boards (8A), (8B), and the wiring length of said flexible wiring board (2) is reduced. Consequently, it is possible to prevent signal delay due to the wiring length. Also, in a semiconductor device having a three-dimensional (3D) structure created by folding the wiring board, it is possible to increase the efficiency of heat dissipation for heat generated inside the laminates by means of shortcut wiring boards (8A), (8B) for said wirings having the same function of the laminates. Also, it is possible to realize double-sided assembly of IC chips on both surfaces of the board, rather than at the solder ball terminal regions for mounting.

[0031]

Application Example 2

Figure 10 is a front view illustrating schematically the constitution of the semiconductor device of Application Example 2 of the present invention. Figure 11 is a front view of the semiconductor device of Application Example 2 mounted on the mounting substrate. The semiconductor device in Application Example 2 is an application example in which the shortcut wiring boards (8A), (8B) of said Application Example 1 are omitted. That is, as shown in Figure 10, said flexible wiring board (2) having said plural semiconductor chips (IC chips) (1) mounted on it at prescribed intervals on the outer principal surface of said flexible wiring board (2) having folding portions (2A) is folded at said double folding portions (2A). As a result, adjacent semiconductor chips (2) mounted on the outer principal surface (first principal surface) of said flexible wiring board (2) are superposed back-to-back, and they are fixed together with adhesive (or adhesive tape) (2B). Said flexible wiring board (2) is further folded at said double folding portions (2A), Au bumps (4) for shortcut wiring connection and lands (4A) for shortcut wiring connection are connected, and the next sets of laminates are layered on. In this way, plural sets of laminates are formed. Said lands (4A) for shortcut wiring connection of wirings having the same function of the laminates and Au bumps (4) for shortcut wiring connection of

the wirings having the same function of the laminates of said plural sets of laminates are electrically connected to reduce the wiring length of said flexible wiring board (2).

[0032]

As shown in Figure 11, in semiconductor device (200) of Application Example 2, solder ball terminals for mounting (common wiring terminals) (7) provided on the inner principal surface (second principal surface) of said flexible wiring board (2) and lands (9A) on assembly substrate (9) for semiconductor device mounting are electrically connected in mounting said device on said mounting substrate (9).

[0033]

In the following, an explanation will be given regarding the method of manufacturing the semiconductor device in Application Example 2. Figure 12 is an outer plan view illustrating the wiring constitution of said flexible wiring board (2). Figure 13 is an inner plan view illustrating the wiring constitution of said flexible wiring board (2). Figure 14 is an overall plan view illustrating the state in which semiconductor chips (1) are mounted on said flexible wiring board (2). Figure 15 is a side view of Figure 14. Figure 16 is a cross section illustrating the state in which one semiconductor chip (1) is mounted on the outer principal surface of said flexible wiring board (2). Figure 17 is a diagram illustrating the state in which flexible wiring board (2) with said semiconductor chips (1) mounting on it is folded to stack said semiconductor chips (1). Figure 18 is an enlarged cross section illustrating the state of connection of the shortcut wiring by folding said flexible wiring board (2) at the double folding portions.

[0034]

In Figures 10-18, (1) represents semiconductor chips (IC chips); (1A) represents the external electrodes of the semiconductor chips (Au bumps on the pads); (2) represents the flexible wiring board (flexible wiring substrate); (2A) represents the double folding portions; (3) represents wiring; (4) represents Au bumps for shortcut wiring connection; 4A represents lands for the shortcut wiring connection; (5) represents via; (6) represents lands for mounting the semiconductor chips; (7) represents solder ball terminals for mounting (external common wiring terminals); (9) represents a mounting substrate; (9A) represents lands for mounting a semiconductor device on the mounting substrate; (10) represents a sealant; (11) represents a flexible board tape; and (12) represents an insulating film (protective film).

[0035]

First of all, flexible wiring board (flexible wiring substrate) (2) is manufactured as shown in Figure 12. As shown in Figure 12, when said flexible wiring board (flexible wiring substrate) (2) is manufactured, wiring is formed on the outer principal surface (first principal surface) of flexible substrate tape (11), with insulating film (protective film) (12) covering it. On the outer principal surface of flexible substrate tape (11) with wiring formed on it as described, wiring (3) for connecting lands (6) for mounting semiconductor chips that have the same function on semiconductor chips (1), lands (4A) for shortcut wiring connection and Au bumps (4) for shortcut wiring connection that connect lands (6) for mounting semiconductor chips and having the same function, of semiconductor chips (1), via (5) for passing said wiring (3) through, and lands (6) for mounting semiconductor chips are formed at their respective positions. On the inner principal surface (second principal surface) of said flexible substrate tape (11), as shown in Figure 13, wiring (3) for connecting lands (6) for mounting semiconductor chips, and having the same function, of semiconductor chips (1), lands (4A) for shortcut wiring connection, as well as Au bumps (4) for shortcut wiring connection and solder ball terminals (7) for mounting are formed.

[0036]

In the method of manufacturing the semiconductor device in Application Example 2, as shown in said Figure 12, flexible wiring board (flexible wiring substrate) (2) is prepared. Then, as shown in Figures 14 and 15, plural semiconductor chips (IC chips) (1) are mounted on lands (6) for carrying semiconductor chips and formed with a prescribed interval on the outer principal surface of said flexible wiring board (2). As shown in Figure 16, semiconductor chips (IC chips) (1) are electrically connected to lands (6) for mounting semiconductor chips by means of external electrodes (Au bumps on the pads) (1A), followed by sealing of the connection region with sealant (sealing resin) (10).

[0037]

As shown in Figure 17, said flexible wiring board (2) having said plural semiconductor chips (1) mounted on it is folded at said double folding portions (2A). As a result, adjacent semiconductor chips (2) mounted on the outer principal surface of said flexible wiring board (2) are superposed back-to-back, and they are fixed together with adhesive (or adhesive tape) (2B). As shown in Figure 17, said flexible wiring board (2) is further folded at said double folding portions (2A), Au bumps (4) for shortcut wiring connection and lands (4A) for shortcut wiring connection are connected, and the next sets of laminates are layered on. In this way, plural sets of laminates are formed.

[0038]

Figures 18(a), (b) show the constitution of said double folded regions. Electrical connection is performed with shortcut wiring portion (2C) of wirings having the same function of the laminates of said plural sets of laminates, so that the wiring length of said flexible wiring board (2) is reduced, and semiconductor device (200) shown in Figure 10 is completed. As shown in Figure 11, for this semiconductor device (200), electrical connection is performed between solder ball terminals (7) for mounting, serving as the external common wiring terminals for wiring having the same function of said laminates, and lands (9A) on assembly substrate (9) for mounting the semiconductor device.

[0039]

As explained above, according to Application Example 2, flexible wiring board (2) that can be folded enables electrical connection among wirings having the same function of the laminates by means of the shortcut wiring portions, and the wiring length of said flexible wiring board (2) is reduced. Consequently, it is possible to prevent signal delay due to the wiring length. Also, in a semiconductor device having a three-dimensional (3D) structure created by folding the wiring board, it is possible to increase the heat dissipation efficiency for the heat generated inside the laminates by means of the shortcut wiring portions for said wirings having the same function of the laminates. Also, it is possible to realize double-sided assembly of IC chips on both surfaces of the board, other than at the solder ball terminal regions for mounting.

[0040]

Application Example 3

The semiconductor device in Application Example 3 of the present invention (semiconductor device (300) or (400)) is another application example similar to said Application Example 2, except that shortcut wiring board (8) in Application Example 1 is omitted here. Figures 19 and 20 illustrate the folding structure ((300) and (400)). The manufacturing method is the same as that of said Application Examples 1 and 2.

[0041]

Application Example 4

Figure 21 includes a plan view, a lateral cross section and a longitudinal cross section illustrating schematically the constitution of the semiconductor device in Application Example 4 of the present invention. Figure 22 is a lateral cross section illustrating the state in which the semiconductor device of Application Example 4 is mounted on a mounting substrate. As shown

in Figure 21, in the semiconductor device of Application Example 4, plural semiconductor chips (IC memory chips) (1) are mounted at prescribed intervals on the outer principal surface (first principal surface) of flexible wiring board (63) having quarter folding portions (2A). The flexible wiring board is double folded at said double folding portions of said flexible wiring board (63), so that semiconductor chips (1) mounted on the outer principal surface of said flexible wiring board (63) are superposed back-to-back, and are fixed together with adhesive (or adhesive tape). Said flexible wiring board (63) is then quarter folded at said quarter folding portions, and the next sets of laminates are layered on. In this way, plural sets of laminates are formed. Electrical connection is made between lands (61) for shortcut wiring connection of wirings having the same function of the laminates of said plural sets of laminates and solder ball terminals (62) for shortcut wiring, and the wiring length of said flexible wiring board (63) is reduced. Relief hole (26) for relieving the folding stress is formed at the center of said flexible wiring board (63).

[0042]

As shown in Figure 22, semiconductor device (500) of Application Example 4 is mounted on said mounting substrate (9), with electrical connection being made between solder ball terminals (common wiring terminals) (7) for mounting, provided on the inner principal surface (second principal surface) of said flexible wiring board (63), and lands (9A) of mounting substrate (9) for semiconductor device mounting.

[0043]

In the following, an explanation will be given regarding the method of manufacturing the semiconductor device in Application Example 4. Figure 23 is an outer plan view illustrating the wiring constitution of said flexible wiring board (63). Figure 24 is an inner plan view illustrating the wiring constitution of said flexible wiring board (63). Figure 25 is an overall plan view illustrating the state in which semiconductor chips (1) are mounted on said flexible wiring board (63). Figure 26 is a side view of Figure 25. Figure 27 is a cross section illustrating the state in which one semiconductor chip (1) is mounted on the outer principal surface of said flexible wiring board (63). Figure 28 includes a plan view, a lateral cross section, and a longitudinal cross section of double folded flexible wiring board (63) carrying said semiconductor chips (1). Figure 29 is a plan view of the quarter folded flexible wiring board (63) carrying said semiconductor chips (1).

[0044]

In Figures 21-29, (1) represents semiconductor chips (IC chips); (1A) represents the external electrodes of the semiconductor chips (Au bumps on the pads); (3) represents wiring; (6)

represents lands for mounting the semiconductor chips (external common wiring terminals); (7) represents a solder ball terminal for mounting; (9) represents a mounting substrate; (9A) represents lands for mounting semiconductor device on the mounting substrate; (10) represents a sealant; (12) represents an insulating film (protective film); (5) represents via; (17) represents minute (buildup) via; (26) represents a relief hole for relieving the folding stress; (61) represents lands for shortcut connection wiring; (62) represents solder ball terminals for shortcut wiring; and (63) represents a flexible wiring board (flexible wiring substrate) with wiring formed on a polyimide tape.

[0045]

First, flexible wiring board (63) is manufactured as shown in Figure 21. As shown in Figures 23 and 24, when said flexible wiring board (63) is manufactured, wiring is formed on flexible wiring board (63), with an insulating film (protective film) covered on it. On the outer principal surface (first principal surface) of flexible wiring board (63), wiring (3) for connecting lands for mounting semiconductor chips that have the same function on semiconductor chips (1), lands (61) for shortcut wiring connection for connecting the lands for mounting semiconductor chips that have the same function on semiconductor chips (1), bumps of solder ball terminals (62) for shortcut wiring, and lands (6) for mounting semiconductor chips are formed at their respective positions. As shown in Figure 24, wiring (3) for connecting the lands for mounting semiconductor chips that have the same function on semiconductor chips (1), lands 61 for shortcut wiring connection, Au bumps (62) for shortcut wiring connection, and solder ball terminals (7) for mounting are formed on the inner principal surface (second principal surface) of said flexible substrate tape (63).

[0046]

In the method of manufacturing the semiconductor device in Application Example 4, as shown in Figures 23 and 24, flexible wiring board (63) is prepared. Then, as shown in Figures 25 and 26, plural semiconductor chips (IC chips) (1) are mounted on the lands for mounting semiconductor chips and formed at prescribed intervals on the outer principal surface of said flexible wiring board (63). As shown in Figure 27, semiconductor chips (IC chips) (1) are electrically connected to the lands for mounting semiconductor chips by means of external electrodes (Au bumps on the pads) (1A), followed by sealing of the connection region with a sealant (sealing resin).

[0047]

When multi-layer wiring is needed, as shown in Figure 27, a buildup system or the like is adopted for flexible wiring board (63), so that it is possible to form a flexible wiring board (63) having both multi-layer wiring portions that allow high-density wiring (the portion from the left side in the figure to immediately before the thinnest portion to the right of center, and the portion that becomes thicker on the right side) and a foldable portion with single-sided or double-sided mono-layer wiring (the thinnest portion positioned between said multi-layer wiring portions).

[0048]

As shown in Figure 28, said flexible wiring board (63) having said plural semiconductor chips (1) mounted on it is double folded at said double folding portions (2A). As a result, adjacent semiconductor chips (1) mounted on the outer principal surface of said flexible wiring board (63) are superposed back-to-back, and they are fixed together with an adhesive (or adhesive tape). In addition, as shown in Figure 29, said flexible wiring board (63) is quarter folded at said quarter folding portions (2A), and the next sets of laminates are layered. In this way, as shown in Figure 21, plural sets of laminates having semiconductor chips (1) superposed back-to-back are formed. Wirings having the same function of said laminates of said plural sets of laminates are electrically connected by means of short circuit electrodes for creating a shortcut, so that the wiring length of said flexible wiring board (63) is reduced.

[0049]

As shown in Figure 22, semiconductor device (500) of Application Example 4 is assembled on said mounting substrate (9), with electrical connection between external electrodes (7) for mounting, serving as common terminals, provided on the inner principal surface (second principal surface) of said flexible wiring board (63) and lands (9A) of mounting substrate (9) for mounting a semiconductor device. Also, when the folding stress is high, a relief hole (26) for relieving the folding stress can be provided. Also, it is possible to use double-sided mounting of the IC chip on the two surfaces of the board, other than at the solder ball terminal regions for mounting.

[0050]

Application Example 5

Figure 30 is a cross section schematically illustrating the state in which the heat absorptive pad of the semiconductor device in Application Example 5 of the present invention is accommodated in the package. Figure 31 is a plan view schematically illustrating the state in which the heat absorptive pad shown in Figure 30 is accommodated in the package. Figure 32 is

a schematic diagram illustrating the constitution of the cooling mechanism with the heat absorptive pad shown in Figure 30.

[0051]

In Figures 30-32, (1) represents semiconductor chips (IC chips); (1A) represents the external electrodes of the semiconductor chips (Au bumps on the pads); (7) represents solder ball terminals for mounting (external common wiring terminals); (26) represents a relief hole for relieving the folding stress; (61) represents lands for shortcut connection wiring; (62) represents solder ball terminals for shortcut wiring; (63) represents a flexible wiring board (flexible wiring substrate) with wiring formed on a polyimide tape; (64) represents a heat absorptive pad; (65) represents a pipe; (66) represents a flow path; (67) represents a fan; (68) represents a heat dissipating part (radiator); (69) represents heat dissipating fins; (70) represents a coolant circulation pump; (71) represents a folded laminated package; and (72) represents a thermoconductive adhesive tape.

[0052]

For the semiconductor device of Application Example 5 of the present invention, laminating is realized by means of cross folding in addition to the bellows folding, double folding and triple [sic; quarter] folding in the aforementioned application examples. As shown in Figures 30 and 31, flexible wiring board (63) (flexible wiring substrate) is quarter folded to laminate semiconductor chips (1). Relief hole (26) for relieving the folding stress is provided at the center of flexible wiring board (63) where the stress is concentrated in cross folding.

[0053]

That is, the semiconductor device has flexible wiring board (63), which has quarter folding portions and relief hole (26) for relieving the folding stress at the center, and which can carry plural semiconductor chips (1) at prescribed intervals on its surface, and plural sets of laminates of semiconductor chips (1) mounted on the outer surface of flexible wiring board (63) and superposed back-to-back when said flexible wiring board (63) is double folded at said double folding portions. Plural semiconductor chips (IC chips) (1) are mounted at the prescribed positions on the outer principal surface of said flexible wiring board (63), and said flexible wiring board (2) is quarter folded at said folding portions (2A), so that semiconductor chips (1) mounted on the outer surface of said flexible wiring board (63) are superposed back-to-back, and are fixed together with adhesive (or adhesive tape) (2B). In addition, said flexible wiring board (63) is quarter folded at said folding portions (2A), and the next set of laminates are layered. In this way, plural sets of laminates are obtained.

[0054]

The thickness of the flexible tape substrate for use in preparing said flexible wiring board (63) may be 75 μm, and the thickness of the Cu wiring may be 35 μm. Wirings having the same function of the laminates of said plural sets of laminates are electrically connected by short circuit electrodes that provide a shortcut, and the wiring length of said flexible wiring board (63) is reduced.

[0055]

As shown in Figures 30 and 31, heat absorptive pad (cooling path) (64) is provided between the laminates with said semiconductor chips superposed. As shown in Figures 30 and 31, said heat absorptive pad (cooling path) (64) is formed with flow path (66). Said heat absorptive pad (cooling path) (64) is fixed by means of thermoconductive adhesive tape (72) between the laminates with said semiconductor chips superposed in a folded stacked laminate package (71).

[0056]

Also, said heat absorptive pad (64) has flow path (66) inside the insulating ceramics or the like used in the IC package. Said flow path (66) goes through pipe (65) and is connected to heat dissipating part (68), and it is filled with water or other liquid. Attachment of heat absorptive pad (64) is performed by means of thermoconductive adhesive tape (72). Also, silicon grease together with an adhesive material can be used for even better performance. Coolant circulating pump (70) force-circulates the internal liquid, and the heat absorbed with heat absorptive pad (64) is transported, with the circulating liquid serving as a medium, through pipe (65) to heat dissipating part (68), and is subjected to forced cooling by fan (67). The liquid cooled in heat dissipating part (68) passes through pipe (65) back to heat absorptive pad (64). Also, a heat pipe, heat dissipating plate, or the like can be incorporated, or a heat sink attached.

[0057]

When multi-layer wiring is needed, as shown in Figure 27, a buildup system or the like is adopted for flexible wiring board (63), so that it is possible to form a flexible wiring board (63) having both multi-layer wiring portions that allow high-density wiring (the portion from the left side in the figure to immediately before the thinnest portion to the right of the center, and the portion that becomes thicker on the right side) and the foldable portion with the single-sided or double-sided mono-layer wiring (the thinnest portion positioned between said multi-layer wiring portions).

[0058]

Said buildup multi-layer wiring portion can be prepared as follows: Wiring (3) is formed with copper or another electroconductive substance on polyimide tape (flexible substrate) (63), followed by laminating insulating photosensitive resin (18). Then, by means of exposure, fine (buildup) via (17) is opened, while the remaining portion is cured to form an insulating layer, and wiring (3) is formed of copper or other electroconductive substance. Consequently, it can be manufactured using the same method as minute (buildup) via (17) even for the foldable portion of a mono-layer wiring.

[0059]

In Application Examples 1-5, the manufacturing method makes use of bare chip assembly by means of Au bumps. However, other manufacturing methods may also be adopted, such as wiring bonding, beam leads, etc. Also, in said application examples, the semiconductor device and its manufacturing method have been explained. However, as can be seen from the aforementioned explanation, the present invention is also applicable to a semiconductor module and its manufacturing method.

[0060]

In the above, the present invention has been explained with reference to application examples. However, the present invention is not limited to the aforementioned application examples. Various modifications are allowed as long as the gist of the present invention is observed.

[0061]

Effect of the invention

The following is a brief account of the effect of the invention disclosed in the present patent application. According to the present invention, in a semiconductor device or semiconductor module with a three-dimensional (3D) structure created by folding a flexible wiring board, short circuit electrodes that provide wiring shortcuts are used for electrical connection so as to reduce the wiring length. Consequently, it is possible to prevent signal delay due to the wiring length. Also, by providing a heat absorptive pad (cooling path) between the laminates when said semiconductor chips are superposed, it is possible to increase the heat dissipation efficiency.

Brief description of the figures

Figure 1 is a front view schematically illustrating the constitution of the semiconductor device in Application Example 1 of the present invention.

Figure 2 is a front view of the semiconductor device of Application Example 1 assembled on a mounting substrate.

Figure 3 is an outer plan view illustrating the wiring constitution of the flexible wiring board in Application Example 1.

Figure 4 is an inner plan view illustrating the wiring constitution of the flexible wiring board of Application Example 1.

Figure 5 is an overall plan view illustrating the state in which the semiconductor chips are mounted on the flexible wiring board of Application Example 1.

Figure 6 is a side view of Figure 5.

Figure 7 is a cross section illustrating the state in which a semiconductor chip is mounted on the flexible wiring board in Application Example 1.

Figure 8 is a plan view illustrating the constitution of the wiring board serving as one and the other shortcut wiring boards in Application Example 1.

Figure 9 is a diagram illustrating the state in which one of the shortcut wiring boards is connected to the wiring of the flexible wiring board in Application Example 1.

Figure 10 is a front view schematically illustrating the semiconductor device in Application Example 2 of the present invention.

Figure 11 is a front view of the semiconductor device mounted on the mounting substrate in Application Example 2.

Figure 12 is an outer plan view illustrating the wiring constitution of flexible wiring board (2) in Application Example 2.

Figure 13 is an inner plan view illustrating the wiring constitution of the flexible wiring board in Application Example 2.

Figure 14 is an overall plan view illustrating the state in which the semiconductor chips are mounted on the flexible wiring board in Application Example 2.

Figure 15 is a side view of Figure 14.

Figure 16 is a cross section illustrating the state in which a semiconductor chip is mounted on the flexible wiring board in Application Example 2.

Figure 17 is a diagram illustrating the state in which the flexible wiring board having semiconductor chips mounted on it is folded in Application Example 2.

Figure 18 is an enlarged cross section illustrating the state in which the flexible wiring board is folded at the double folding portions of the flexible wiring board in Application Example 2.

Figure 19 includes a front view, plan view, and side view illustrating schematically the constitution of the semiconductor device in Application Example 3 of the present invention.

Figure 20 is a front view schematically illustrating the constitution of the semiconductor device in Application Example 3.

Figure 21 includes a plan view, a lateral cross section and a longitudinal cross section illustrating schematically the constitution of the semiconductor device in Application Example 4 of the present invention.

Figure 22 is a lateral cross section of mounting of the semiconductor device on the mounting substrate in Application Example 4.

Figure 23 is an outer plan view illustrating the wiring constitution of the flexible wiring board in Application Example 4.

Figure 24 is an inner plan view illustrating the wiring constitution of the flexible wiring board in Application Example 4.

Figure 25 is an overall plan view illustrating the state in which semiconductor chips are mounted on the flexible wiring board in Application Example 4.

Figure 26 is a side view of Figure 25.

Figure 27 is a cross section illustrating the state in which a semiconductor chip is mounted on said flexible wiring board (when a multi-layer wiring is adopted) in Application Example 4.

Figure 28 includes a plan view, a lateral cross section and a longitudinal cross section of the double folded flexible wiring board having semiconductor chips mounted on it in Application Example 4.

Figure 29 is a plan view of the quarter folded flexible wiring board having semiconductor chips mounted on it in Application Example 4.

Figure 30 is a cross section schematically illustrating the state in which the heat absorptive pad of the semiconductor device is accommodated in the package in Application Example 5 of the present invention.

Figure 31 is a plan view schematically illustrating the state in which the heat absorptive pad is accommodated in the package in Application Example 5.

Figure 32 is a schematic diagram schematically illustrating the constitution of the cooling mechanism using the heat absorptive pad in Application Example 5.

Explanation of reference symbols

| | |
|---|---|
| 1 | Semiconductor chip (IC chip) |
| 1A | External electrodes of semiconductor chip |
| 2 | Flexible wiring board |

| | |
|---|---|
| 2A | Folding portion |
| 2B | Adhesive for semiconductor chip |
| 2C | Shortcut wiring connecting portion |
| 3 | Wiring |
| 4 | Au bump for shortcut wiring connection |
| 4A | Land for shortcut wiring connection |
| 5 | Via |
| 6 | Land for mounting semiconductor chip |
| 7 | Solder ball terminal for mounting |
| 8A, 8B | Shortcut wiring board |
| 9 | Mounting substrate |
| 9A | Land for mounting of semiconductor device |
| 10 | Sealant |
| 11 | Flexible substrate tape |
| 12 | Insulating film (protective film) |
| 17 | Minute (buildup) via |
| 18 | Insulating photosensitive resin |
| 22 | Adhesive tape |
| 23 | Solder |
| 26 | Relief hole for relieving the folding stress |
| 61 | Land for shortcut wiring connection |
| 62 | Solder ball terminal for shortcut wiring |
| 63 | Flexible wiring board |
| 64 | Heat absorptive pad |
| 65 | Pipe |
| 66 | Flow path |
| 67 | Fan |
| 68 | Heat dissipating part (radiator) |
| 69 | Heat dissipating fins |
| 70 | Coolant circulating pump |
| 71 | Folding laminated package |
| 72 | Thermoconductive adhesive tape |

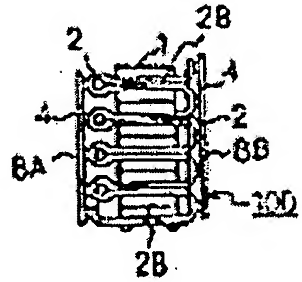



Figure 1

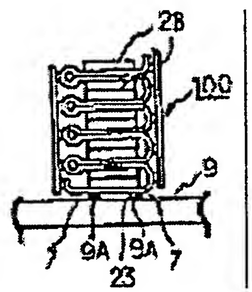
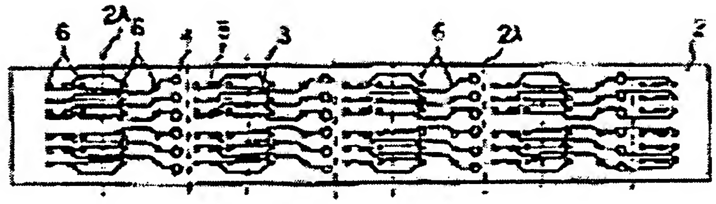



Figure 2

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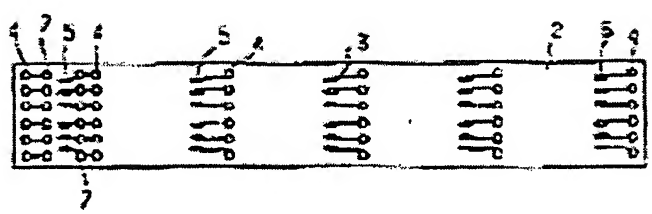



Figure 4

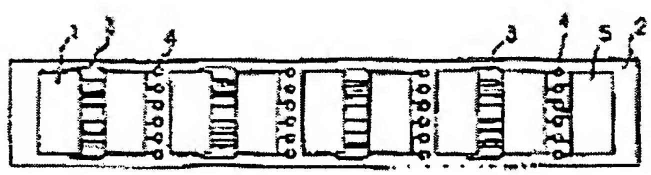



Figure 5

Figure 6

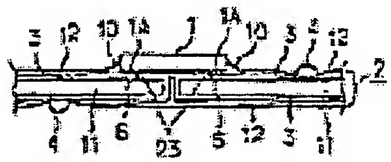


Figure 7

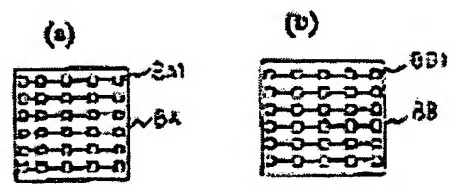


Figure 8

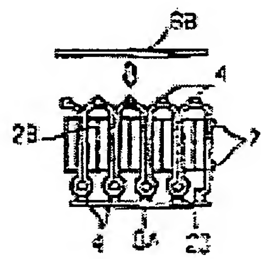


Figure 9

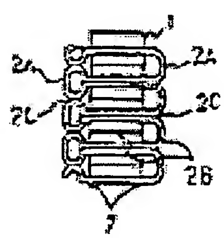


Figure 10

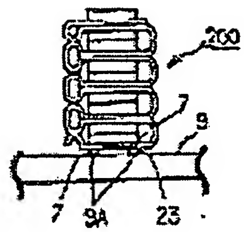



Figure 11

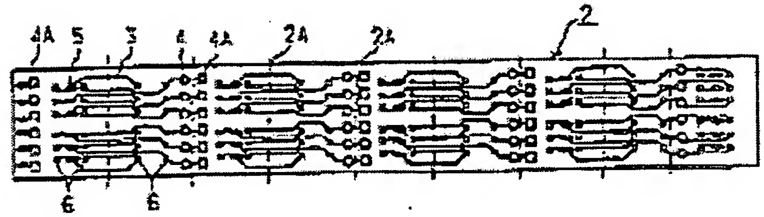



Figure 12

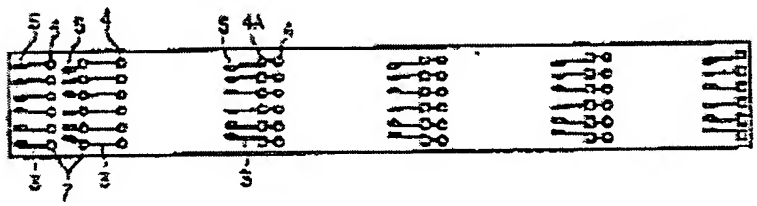
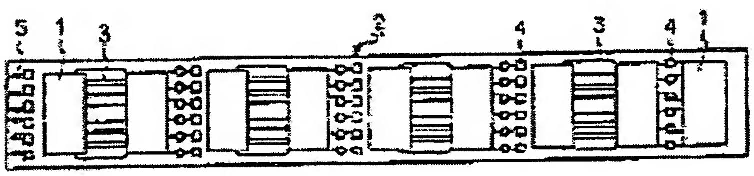



Figure 13

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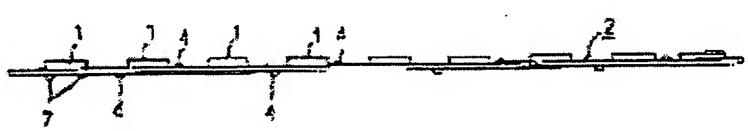



Figure 15

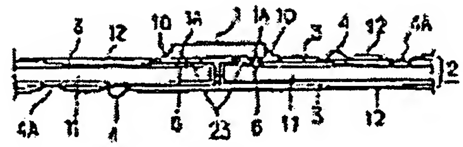
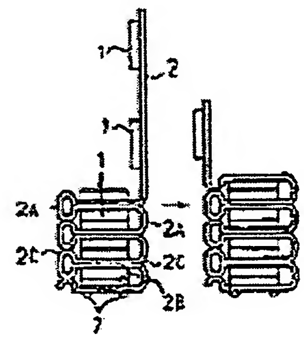


Figure 16



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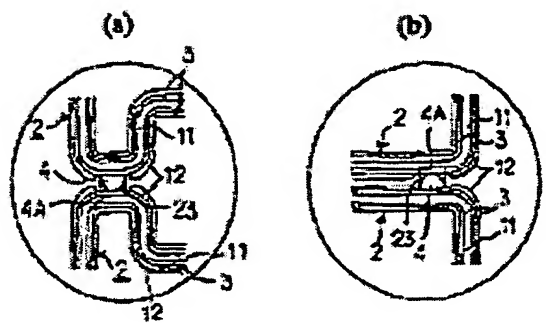

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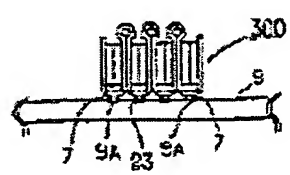
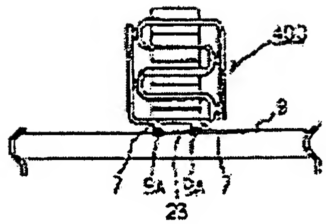


Figure 19

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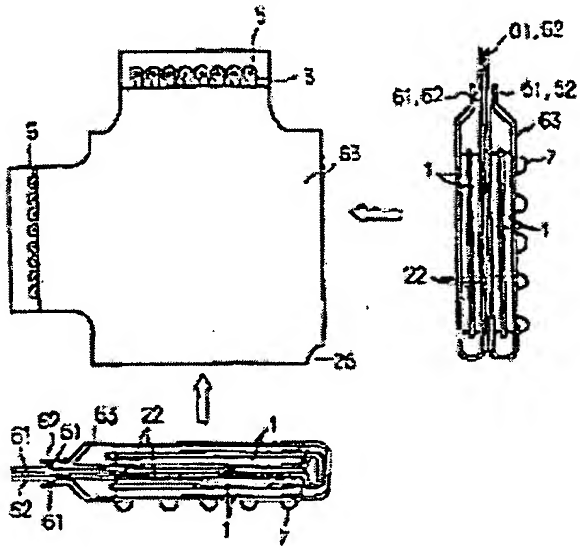



Figure 21

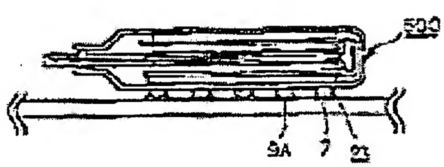



Figure 22

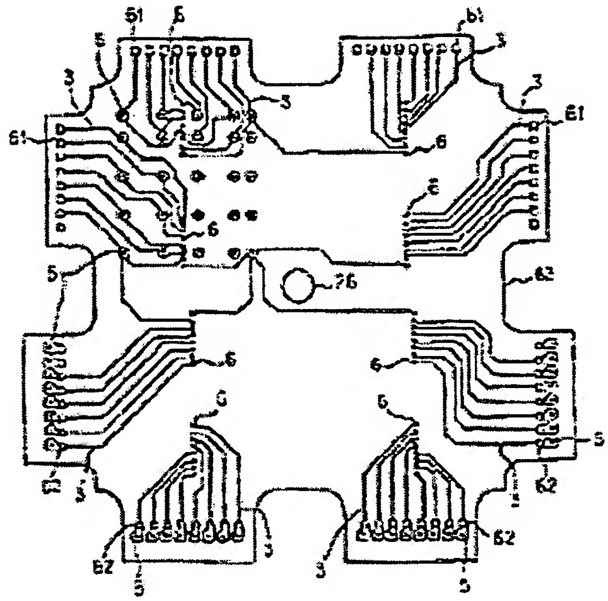
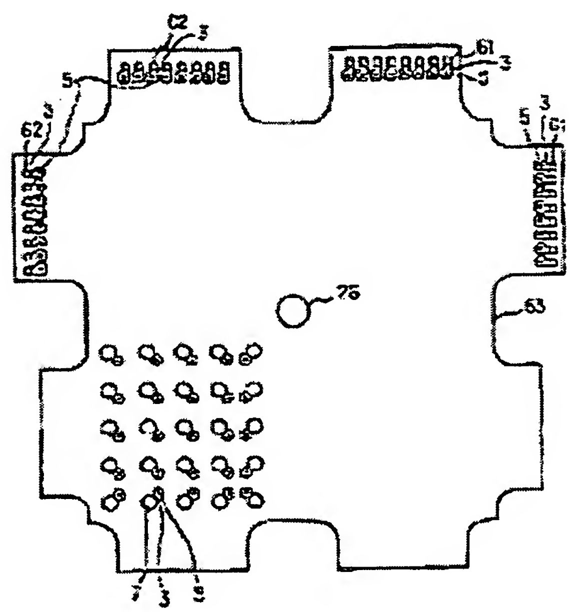


Figure 23



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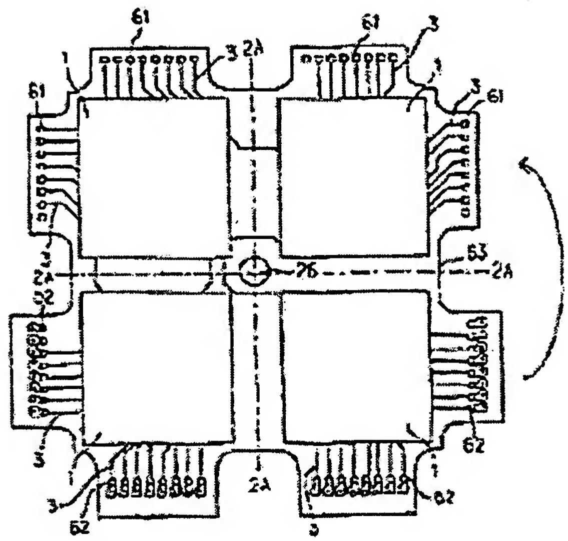

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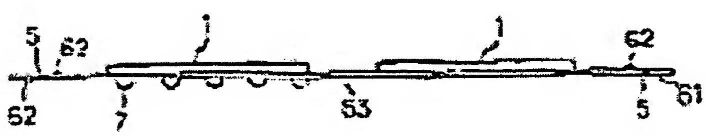

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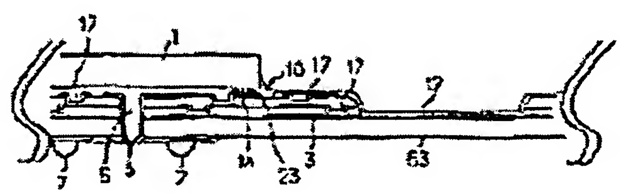
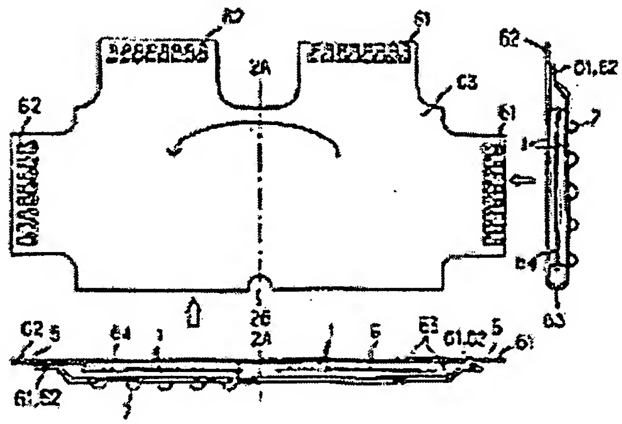


Figure 27



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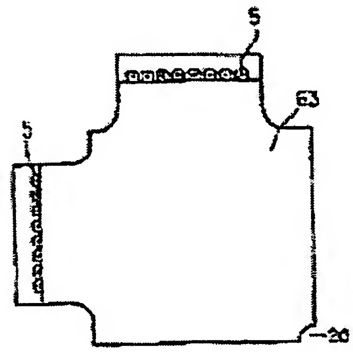

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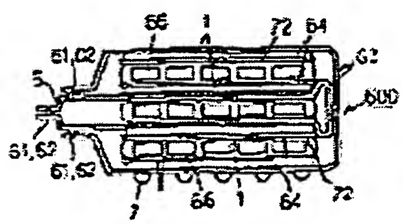

Figure 30

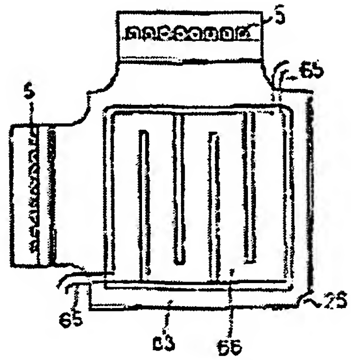


Figure 31

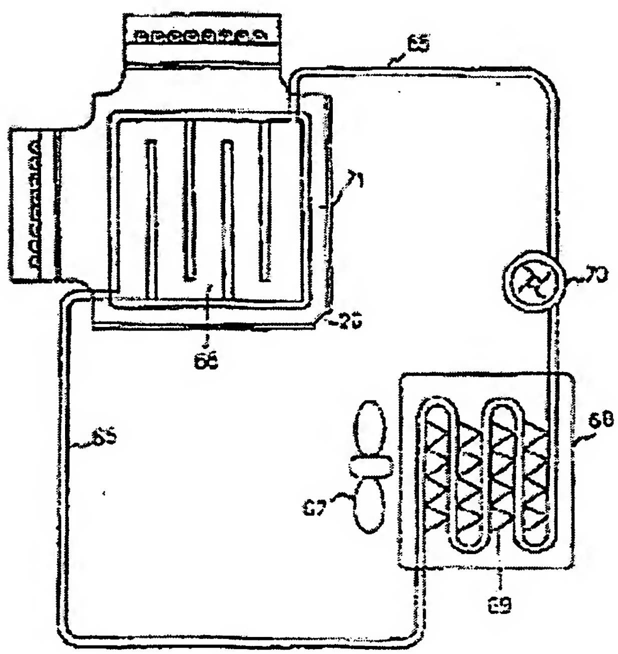


Figure 32